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Silicon Nanowire Field-effect Chemical Sensor

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BIOS
lab on a chip group

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SILICON NANOWIRE FIELD-EFFECT CHEMICAL SENSOR

DISSERTATION

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To My Husband

Contents

Chapter 1

Introduction

1.1 Project aim and description

The project "Design and optimization of silicon nanowires for chemical sensing" is part of blue bolus chip (BBC) project, funded by a private foundation in the Netherlands. The goal of the BBC project is to develop a "smart pill" that is small enough to be ingested by a patient and is capable of sampling intestinal fluid and performing a series of diagnostic tests for cancer detection via hypermethylated DNA. Upon ingestion, the smart pill travels to the upper large intestine, where intestinal fluid is sampled by a miniaturized lab-on-a-chip (LOC) system (Fig. 1.1a, b). The sample fluid is mixed with a pre-stored salt solution and subsequently the sample DNA is purified and concentrated in a separation chamber. The captured DNA molecules are then transported to the detection stage, where target cancer DNA molecules hybridize selectively to the complimentary DNA molecules attached to the surface of the silicon nanowire (Si-NW) sensors. When a positive detection event occurs, the integrated electronics provides the patient an indication by pumping out a blue pre-stored dye into the bowel, which can be easily observed after defecation or by wireless transmission to a nearby cellular telephone. The five primary BBC "smart-pill" system components are shown schematically in Fig. 1.2.

The primary aim of this project is to develop the detection stage (Fig. 1.2) of the smart-pill system using an all electrical label-free biosensing system that can be easily integrated with conventional interface electronics. In general, label-free biosensors directly detect the hybridization of an affinity complex and can be done by a variety of methods including optical, mechanical, and electrochemical

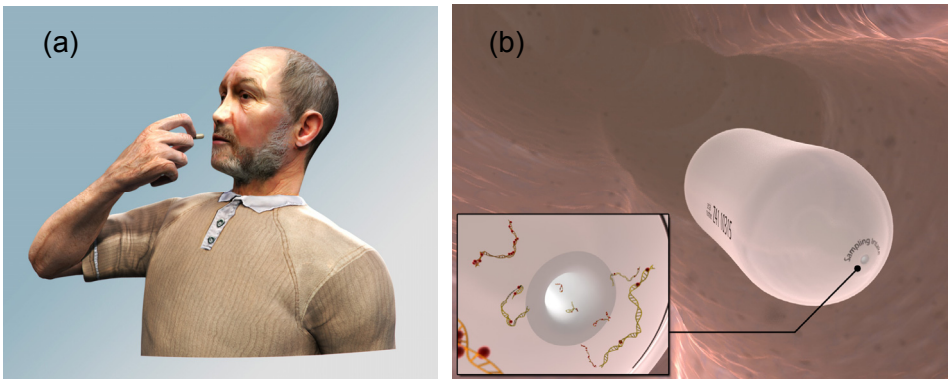

Figure 1.1 (a) Ingestion of the smart pill and (b) sampling in intestinal fluid.

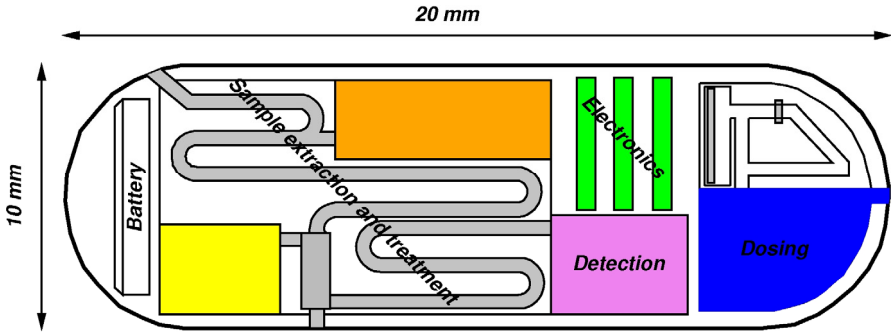

Figure 1.2 Schematic description of smart-pill.

techniques. In this project, we explore the sensing limitations of Si-NWs to detect probe-target binding based on surface charge modulation. Si-NWs have been reported to be capable of providing highly sensitive label-free biomolecular sensing that can be manufactured into dense arrays and additionally provide a real-time electrical output that can be easily integrated with conventional data recording equipment. However, the majority of these reports have not systematically studied the sensing limitations and critical device characteristics.

The four main goals of the project are:

1) Fabrication, design and optimization of Si-NWs using conventional fabrication techniques that result in well defined NW structures with reproducible and well-defined surface.

2) Modeling the electrochemical and electrical behavior of the manufactured Si-NW sensors.
3) Surface characterization, and functionalization of silicon surfaces with appropriate molecular probes.
4) Developing an integrated LOC/Si-NW biosensing platform.

1.2 Outline of the thesis

Chapter 2 gives a general review on the recent developments in Si-NW research, including their electrical properties, various fabrication techniques, and some different sensor applications.

In Chapter 3, we present a low-cost top-down silicon nanowire fabrication technology that requires only conventional microfabrication processes including microlithography, oxidation and wet anisotropic plane-dependent etching. The advantages of the new fabrication technology are discussed and demonstrated with multi-scale microscopy images.

Chapter 4 introduces other important considerations in Si-NW device fabrication, which we call advanced fabrication techniques. The three main aspects we consider are impurity doping, ohmic electrical contact formation and the effect of channel depletion during Si/SiO_2 gate oxide formation.

The topic of Chapter 5 is the electrochemical/electrical modeling of Si-NWs in solution. A two-dimensional (2D) analytical model of the conductance for triangular Si-NWs is presented. The simplified physical expressions introduced in this chapter fit well with the measured *IV* characteristics. A three-dimensional (3D) finite-element TCAD model of the Si-NW devices has been developed and sensor sensitivity has been assessed with different parameters, e.g. NW size, doping, gate oxide thicknesses and noise. Comparisons between the 2D analytical/3D numerical models and measured conductance as a function of front-gate voltage are presented.

Chapter 6 introduces the nanoISFET for pH sensing. A comparison between the nanoISFET and the conventional ISFET is presented, describing the similarities and differences in device structures and working principles. Extensive electrochemical testing of fabricated nanoISFETs has been conducted. Three variations of a SiO_2 gate-oxide and an ALD Al_2O_3 gate-oxide have been deposited on the nanoISFETs and titration experiments were used to assess the pH behavior and sensitivity. A comprehensive analytical model of the nanoISFET sensor is

discussed that utilizes the well-established Site-Binding Model (SBM) accompanies the experimental results.

In Chapter 7, an integrated lab-on-a-chip (LOC) label-free biosensing platform is presented that consists of a silicon nanowire (Si-NW) device chip, integrated with microfluidic channels molded in polydimethylsiloxane (PDMS) layer for small volume sample transport. The functional biosensing platform is demonstrated with pH sensing experiments. Finally, chapter 8 gives the summary of present work and an outlook for future research.

Chapter 2

Silicon Nanowire Field-effect Sensor

In this chapter, Si-NWs are introduced together with their unique properties. The schematic and physics of Si-NW as field-effect transistor (FET) are then explained in section 2.2. Due to their small size, there has been some effort in fabricating them either by bottom-up or top-down methods. Several interesting fabrication techniques are summarized in section 2.3. In the end, applications of Si-NWs as various FET sensors are presented, e.g. pH sensor, biosensor, flow sensor.

2.1 Introduction

A NW is an extremely small structure, typically with diameters on the order of few nanometers up to 100 nm, where 1 nm = 10^{-9} m. NWs have many interesting properties that are not significant in bulk materials with the same composition. Some of these properties can also be seen in other nanostructures (e.g. nanoparticles, nanotubes and nanochannels)[1]. Compared with nanoparticles (zero-dimensional nanostructures), NWs provide a better model system for investigating the dependence of electronic transport, optical, and mechanical properties on size confinement and dimensionality[2]. One-dimensional structures also represent the minimum dimensionality for electrical conduction.

Nanowires have distinctive electrical, thermal, photonic and mechanical properties compared with their bulk counterparts as demonstrated by theory and numerous experiments[3-6]. The reduction in device dimensions is now reaching the regime where classical physics becomes invalid. However, NWs with widths above ~50 nm can be described classically, but can also exhibit interesting physical behavior due to the large surface-to-volume ratio (SVR). The NW devices used throughout this thesis have dimensions in the 50 nm to 200 nm range and their behavior is described using classical electrostatic and semiconductor physics theory. The size and shape of nanomaterials play an important role in the fabrication and application of NWs and a lot of attention has been paid to the fabrication of small and stable NWs. Since the minimum dimension that a material can be made into a NW depends heavily on the fabrication technique. Presently, a NW can be realized as small as a single strand of atoms suspended in ultra high vacuum, with the length of several atoms[7], however these atomic-scale devices are far away from being used for practical applications despite the staggering pace at which the manipulation techniques and functional understanding are moving.

Semiconductor NWs have been the focus of technology development both in fabrication and applications because of their unique semiconducting properties and wide application in integrated circuit (IC) technology. Nanowire devices have been demonstrated as ultrasensitive molecular sensors for detection of biological and chemical samples. The physical properties limiting sensor devices fabricated in planar semiconductors can be readily overcome by exploiting nanoscale FETs[8]. Si

nanowire field effect transistors (FETs) were reported to detect biomolecules with high sensitivity and selectivity[8-10].

2.2 Si-NW sensor basics

Si-NW chemical sensors operated as field-effect transistors (FET) are currently the most commonly used structures. Generally, a Si-NW FET device consists of an either p-doped or n-doped Si-NW connected to two metal contacts, named source (S) and drain (D), as shown in Fig. 2.1a. The thin Si-NW body is electrically isolated from the silicon substrate by a buried oxide (BOX) layer, and the front-gate (FG) and back-gate (BG) contacts are used to control the conductance G of the Si-NW electrostatically across the front-oxide (FOX) and/or BOX layers respectively. Figure 2.1b depicts an equivalent electrical circuit diagram of a Si-NW chemical sensor with typical electrical and electrochemical biasing and measurement configuration. The system consists of the Si-NW field-effect device, a reference electrode that provides a solution interface to the FG, a current measurement device, and three voltage sources v_{ds}, V_{fg} and V_{bg}. The lumped capacitors shown in Fig. 2.1b are C_d representing the differential capacitance of the interface between the solution and the FOX layer, and C_{bd} and C_{sb} representing the electrical capacitances between the Si-NW and the substrate silicon separated by the BOX layer. Capacitors C_{fo} and C_{bo} represent the FG and BG capacitance and are used to control the device conductance, which is represented as resistance R_{NW}.

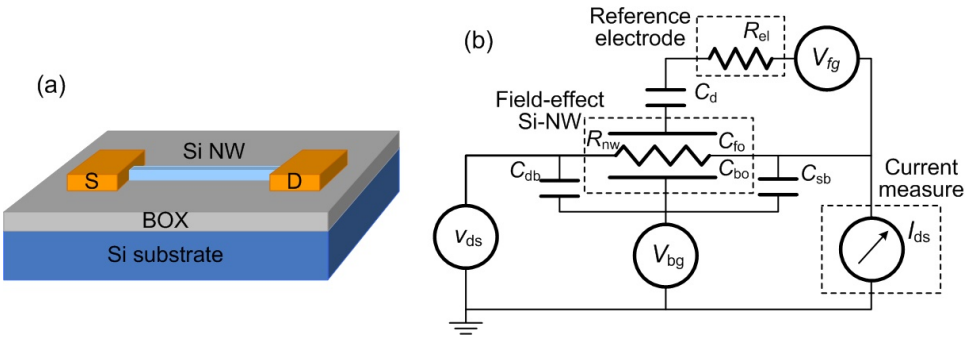

Figure 2.1 (a) Structure of a Si-NW device (b) Equivalent electrical circuit model of the Si-NW chemical sensor with typical electrical biasing and measurement system.

The FOX layers of the multi-gate structure have approximately the same thickness and are considered to be symmetric with respect to the FG. Since the BOX layer is typically much thicker (> 10×) than the FOX layer, BG biasing is much larger compared to the FG to produce a similar field-effect. A small voltage v_{ds} (either AC or DC) is normally applied to the drain and source, and current through the Si-NW is measured. The advantage of using an AC voltage is that a small bandwidth measurement can be performed using a lock-in-amplifier[8, 10]. However, the frequency of the driving signal should be low in order to have minimum influence of the low-pass filter formed at the input of the transconductance readout circuit due to C_{sb}.

The silicon field-effect devices have three distinct operation regimes where the accumulation, depletion and inversion space charge regions are created in the semiconductor layer by controlling the potential ψ_s of the silicon surface. In the depletion regime, bound ionized impurity charge Q_d dominates, while in the accumulation and inversion regimes free charge (Q_a and Q_i, respectively) at the surface dominates. Since the Si-NWs are gate voltage controlled devices, it is useful to consider first the ideal voltage-controlled charge modulation behavior of the metal-oxide-semiconductor (MOS) system. The electrolyte-oxide-semiconductor (EOS) system will be described in detail in Chapter 5. Figure 2.2 shows the total silicon charge $|Q_s|$ of a single MOS surface, as V_{fg} is varied from small negative to small positive voltages, where an exact solution of Poisson's equation[11] is plotted for three different doping concentrations. The inset shows ψ_s as a function of V_{fg} across the FOX layer with thickness t_f, where ψ_s varies rapidly with V_{fg}, in the depletion region. However, a large V_{fg} is required to produce a small change in ψ_s, in the accumulation and inversion regions, which is important for device sensitivity. For negative V_{fg}, majority carrier accumulation occurs and increases sharply with V_{fg}, more or less independent of the impurity doping concentration. For small positive V_{fg}, the silicon body is partially depleted and strongly dependent on the silicon body doping. For larger V_{fg}, an inversion charge layer is formed and is strongly dependent on the body doping concentration and silicon body thickness[12]. In all three regions the device current-voltage and sensitivity characteristics are very different.

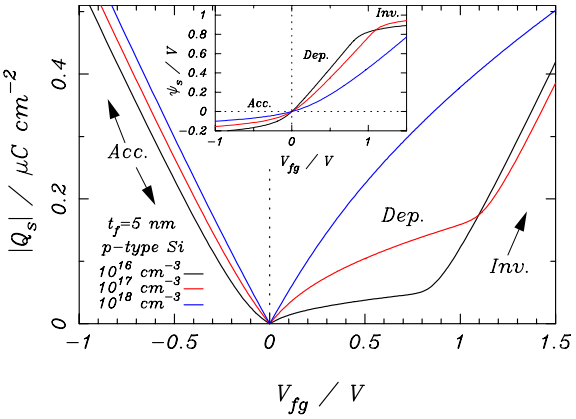

Figure 2.2 Total silicon charge $|Q_s|$ of a single planar MOS surface as a function of V_{FG} in the accumulation (Acc.), depletion (Dep.), and inversion (Inv.) regions with varying doping concentrations. Inset: surface potential ψ_s as a function of V_{fg}.

In this simplified description, effects of fixed-oxide and silicon/oxide interface trapped charges have been neglected and $V_{fg} = 0$ is defined as the flat-band potential where $\psi_s = 0$. The MOS flat-band voltage is $V_{fb} \equiv V_{fg}(\psi_s = 0) = \phi_{MS} - Q_{tfo}/C_{fo}$, where ϕ_{MS} is the work function difference between the metal front-gate contact and the silicon layer, Q_{tfo} is the total trapped and fixed charges associated with the FOX layer[13] and C_{fo} is the capacitance per unit area of the FOX layer. Additionally, it should be noted that in the previous description, any depletion or accumulation region at the back-oxide Si-NW interface due to the back-gate contact has been neglected for partially-depleted operation, which can be important for low channel doping levels and gate potentials near the threshold voltage[14].

Si-NW FET devices are very different than their planar predecessors. There are two important differences that are important for chemical and biochemical sensors. The first important difference is an increase in SVR due to the multi-gate structure. The large SVR of NWs renders them extremely sensitive to surface species such that small detection volumes are possible. With the same amount of surface charges present, $\Delta G/G_o$ (G_o is the bias conductance of Si-NWs) is higher with reducing the size of NW. For Si-NWs, scaling the width from 200 nm down to 50 nm resulted in an estimated 20× increase in sensitivity to large surface potential changes[15]. Figure 2.3 shows an example of the relationship between $\Delta G/G_o$ and the

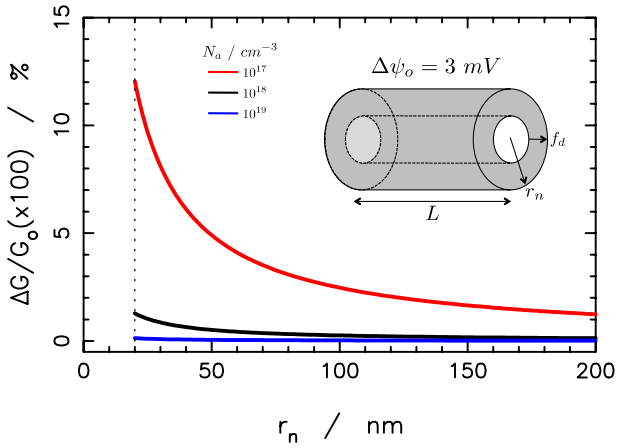

Figure 2.3 Calculated relationship between the normalized conductance $\Delta G/G_o$ and the radius of the circular nanowire for a FOX surface potential change $\Delta\psi_o$ = 3 mV, t_f = 5 nm, L = 10 μm, doping dependent mobility μ_b and various impurity doping concentrations.

radius of a circular nanowire operated in the depletion region[i]. It should be noted that this general relationship is similar for other cross-sectional shapes.

From Fig. 2.3 the normalized conductance shows a strong dependence on both radius and impurity doping concentration. An interesting feature of this simple analytical model is the fact that very large nanowires (r_n = 200 nm) with N_a = 10^{17} cm^{-3} have similar or greater normalized conductance than heavily doped devices (N_a = 10^{18} cm^{-3} - 10^{19} cm^{-3}) with very small dimensions (r_n = 20 nm).

Another important property of a nanoscale potentiometric sensor is that a smaller number of molecules can generate the same surface potential change compared to macroscale sensors. For example, consider that a particular surface attachment protocol results in surface coverage density of κ = 1 probe molecule per 2 nm^2 results in a surface potential change $\Delta\psi_o$. A circular nanowire with radius r_n

[i] The depletion region conductance is calculated with $G = \pi q \mu_b N_a L^{-1}(r_n - f_d)^2$, where majority carrier hole mobility is $\mu_b = \mu_{max} + \mu_{max} - \mu_{min} \Big/ 1 + \left(N_a / N_{ref}\right)^{\alpha}$ with μ_{min} = 44.9 cm^2 V^{-1} s^{-1}, μ_{max} = 470.5 cm^2 V^{-1} s^{-1}, N_{ref} = 2.23×10^{17} cm^{-3} and α = 0.719; L is the device length, r_n is the radius and the depletion distance function is:

$$f_d \approx \left(\left(t_f \varepsilon_{Si} / \varepsilon_{ox} \right)^2 + 2\varepsilon_{Si}\varepsilon_{ox}\psi_o / qN_a \right)^{1/2} - t_f \varepsilon_{Si} / \varepsilon_{ox} \text{ with } \varepsilon_{Si} = 11.9 \text{ and } \varepsilon_{ox} = 3.9.$$

= 25 nm and length L = 10 μm has a surface area of $A_s = 2\pi r_n L \approx 1.6\times10^6$ nm^2, and the total number probe molecules on the nanowire is then $N_n = \kappa A_s \approx 8 \times 10^5$ probe molecules. If we consider a macroscale sensor with surface area A_s = 5 μm × 10 μm, then the number of probe molecules is $N_m \approx 2.5\times10^7$ probe molecules. The nanoscale sensor has a large reduction, $N_m/N_n \approx 32\times$, in the number of probe molecules required to produce the same $\Delta\psi_o$ and the device ΔG. Therefore, if we assume the same hybridization efficiency then the nanoscale sensors can offer significantly improved sensitivity. It should be noted that for low concentrations of analytes (e.g. sub-picomolar), the time that is required to transport the target molecules to the nanoscale sensors with small surface areas would be impractically long (hours to days)[16]. Thus effective collecting of target molecules on the NW surface is needed in order to take advantage of the scaling effect[17-19].

2.3 Fabrication techniques

The Si-NW fabrication techniques can be classified into two categories: bottom-up and top-down techniques. In this section, a brief description of common bottom-up fabrication techniques are presented, and followed by a detailed review on top-down fabrication methods.

2.3.1 Bottom-up fabrication

The bottom-up approach assembles molecules and small solid structures from atoms that are combined into a large variety of shapes and functions. A large number of materials have been successfully synthesized into nanostructures over the past decade[20, 21]. The bottom-up technique can be traced back to the early 1960s, when Wagner et al.[22] used the vapor-liquid-solid (VLS) mechanism for crystal growth of silicon whiskers. The dimensions of the whiskers they made were as small as 100 nm. The VLS process involves two main steps, as shown in Fig. 2.4a: 1) the formation of a small liquid metal droplet, typically Au, and 2) the alloying, nucleation, and growth of the NW. The growth process typically occurs in the temperature range of 300 – 1100 °C. It starts with the dissolution of gaseous reactants in nano-sized liquid catalyst droplets, which causes the liquid to be supersaturated with Si. Then the wire grows by precipitation of Si from the droplet. The diameter of the NW can be made below 5 nm, and is limited by the minimum

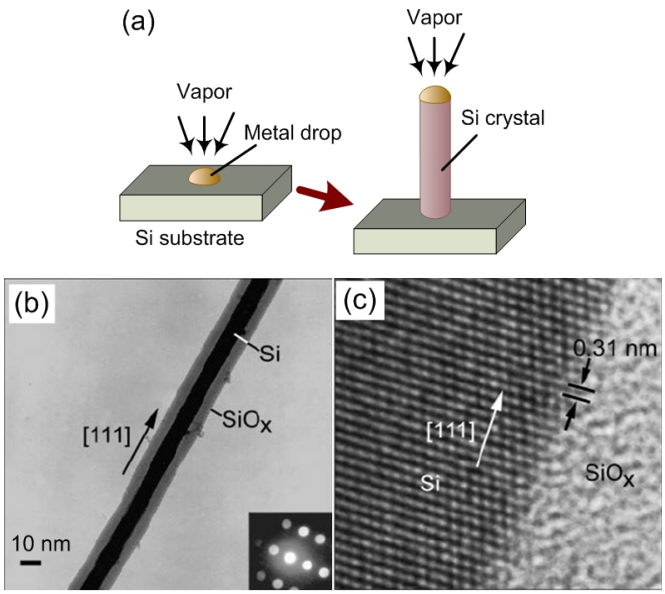

Figure 2.4 (a) The growth mechanism of VLS, (b) (c) TEM images of a high quality Si-NW[27].

diameter of the liquid metal droplet, the growth temperature and pressure[23]. Figure 2.4b, c show high-resolution transmission electron microscope (TEM) images of VLS grown Si-NWs, with crystalline structures. Other techniques include the vapor-solid (VS) process[24], electrochemical deposition[25, 26], and solution growth are also widely used for growth of NWs.

Bottom-up nanofabrication is in principle simple and provides high quality materials, and can be applied to various materials such as Si[23, 27, 28], Ge[27], GaN[29], Au[30, 31] and ZnO[32, 33]. However, current manufacturing methods do not provide controlled growth into high-density ordered arrays and typically requires transfer and assembly of devices on separate substrates. The approaches implemented for assembly of NW devices include fluidic assembly (Fig. 2.5a)[34], the Langmuir-Blodgett method[35], spin coating on the substrate[36], contact printing[37, 38], electrical field assembly[39], and dielectrophoresis assembly (DEP) (Fig. 2.5b)[40]. After assembling the NWs on the substrate using the previously described methods, they need to be located with a scanning electron microscope (SEM), followed by electrical contact formation using an appropriate metal layer. These methods

require a long time to achieve contact alignment and encounter difficulties in controlling the doping and contact properties[41]. Dielectrophoresis assembly provides high-yield assembly of NWs over patterned electrodes sites. However, the robustness of the contact through the van der Waals force remains a concern. Therefore, suitable methods for accurate nanowire alignment are lacking, and electrical contact formation is problematic, making it difficult to construct functional device arrays[42].

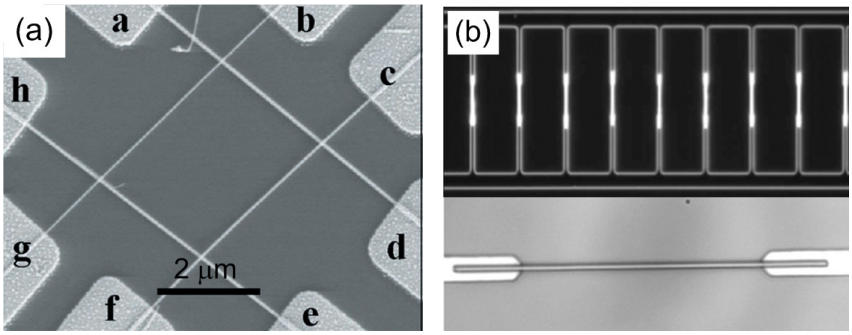

Figure 2.5 Assembled results from (a) fluidic and (b) DEP assembly.

2.3.2 Top-down fabrication

Top-down fabrication technology is the standard technique for semiconductor manufacturing, and is based on standard microfabrication methods consisting of deposition, patterning and etching. NWs from multiple materials, e.g. Si[43-45], Pt[43], Au[46, 47] and TaO_2[48], have been realized. Conventional top-down nanopatterning techniques, such as deep-UV photolithography[49] is currently the standard for semiconductor manufacturing. Advanced nanopatterning, such as electron-beam lithography (EBL) and focused-ion-beam (FIB) lithography can write feature sizes below 10 nm, however, the main drawback is slow and not practical for wafer-scale fabrication. In this section, alternative fabrication methods are introduced.

a) Nanoimprint lithography (NIL)

Nanoimprint lithography is a low cost mass manufacturing technology that uses compression molding of thermoplastic polymers[50] or photo curable liquid resists[51] to fabricate nanometer scale patterns[52]. The two basic steps are shown in Fig. 2.6a. The first step is the imprint step in which a mold with nanostructures on its surface

is pressed into a thin resist cast on a substrate, followed by removal of the mold. This step creates a thickness contrast pattern in the resist. The second step is the pattern transfer where an anisotropic etching process (O_2 plasma etching) is used to remove the residual resist in the compressed area. Nanostructures can be formed later by either direct pattern transfer to the substrate by etching or liftoff. Since this process does not use any energetic beams, the resolution is not limited by the effects of wave diffraction, scattering and interference in a resist, and backscattering from the substrate. Superlattice nanowire pattern transfer (SNAP) as an alternative NIL method was introduced by Heath group[43, 53], which can produce ultrahigh-density arrays of aligned metal and semiconductor NWs and NW circuits. Figure 2.6b shows the Si-NW arrays fabricated by SNAP. The disadvantage with NIL is the replication stamp fabrication is complicated and large area wafer-level patterning and defect control remains problematic.

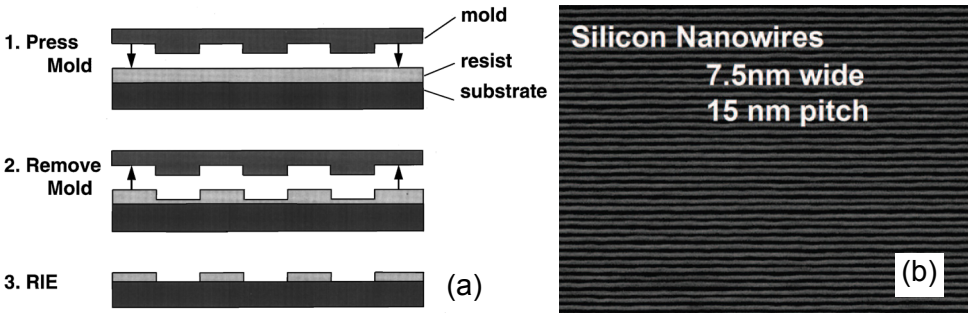

Figure 2.6 (a) Schematic of Si-NWs fabricated by NIL[54] (b) Si-NW arrays with width of 7.5 nm[53].

b) Spacer patterning

Spacer lithography (or commonly referred to as size reduction lithography) uses a sacrificial layer and etching steps to achieve dimensions down to 6.5 nm[55-57]. It overcomes the limits of conventional lithography and the minimum sized features are finished not by photolithography but by the thickness of the sacrificial layer. Therefore, the spacer lithography technology yields extreme narrow and uniform features. By conformally depositing a material (silicon oxide or silicon) that has a different etching property over a lithographically defined sacrificial sidewall and selectively removing the sacrificial material, the sidewall material is preserved and

can serve as nanopattern mask for further processing (Fig. 2.7a). Figure 2.7b shows Si-NW arrays with lateral dimensions of 20 nm fabricated with spacer patterning. This technology is already used to pattern silicon-fin structures for MOSFETs and CMOS FinFET with excellent behavior[57]. However, the fabrication of high density features with well controlled dimensions requires expensive and complicated etching techniques.

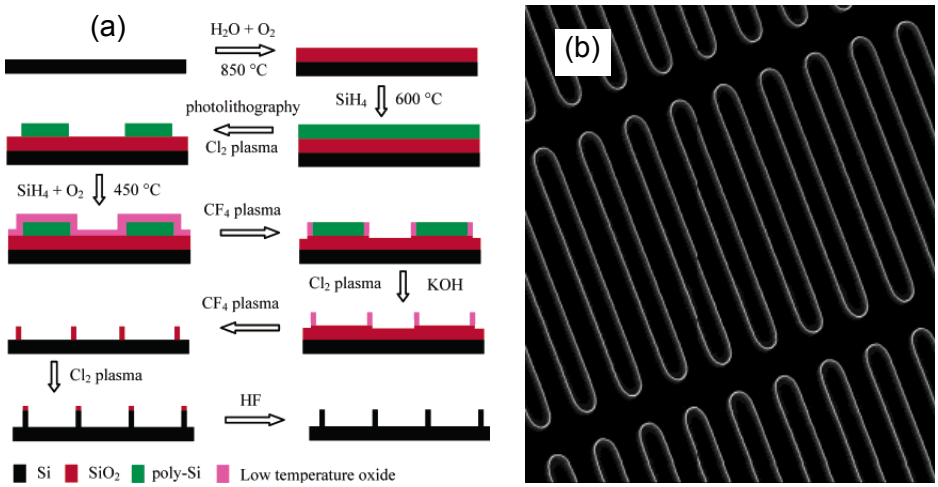

Figure 2.7 (a) Schematic of spacer lithography process (b) SEM images of 20 nm Si-NW array.

c) Nanostencils

The nanostencil technique is used for the generation of submicrometer and nanopatterns without photolithography, thus a resistless process[58]. It makes use of a thin silicon nitride membrane with circular, rectangular, or line-shaped apertures fabricated by electron beam[59] or FIB[60]. This membrane serves as a shadow mask for the deposition of various materials. As shown in Fig. 2.8a, the size of deposited nanostructure depends on the dimension of the stencil aperture and source, distance between source and substrate, and the gap, which in all cases result in larger features than the stencil apertures. Fig. 2.8b also shows the size comparison between a stencil aperture (above) and fabricated NW (below). Metallic NWs with width down to 15 nm have been realized[59]. However the shadow-mask evaporation is accompanied by gradual aperture clogging. The masks then need to be cleaned or

replaced. Suppressing the adhesion of the deposition materials can be achieved by a self-assembled monolayer coating on the nanostencils[61].

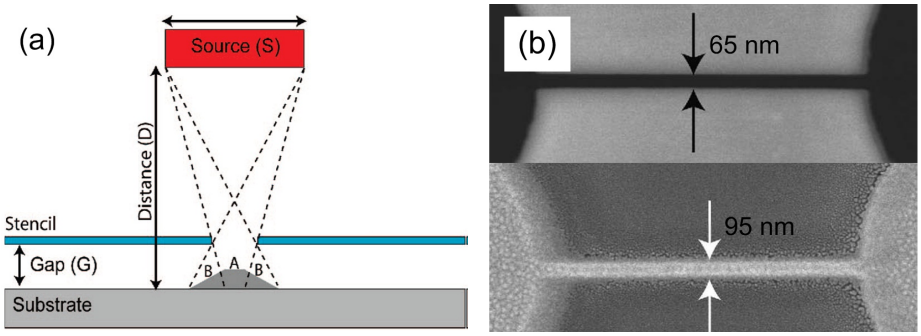

Figure 2.8 (a) Nanostencil fabrication process and (b) size comparison between stencil aperture and fabricated NW[60].

d) Deposition and etching under angle (DEA)

Low-cost top-down NW fabrication can be realized by DEA, which uses a combination of angled thin-film deposition and etching of a metal layer in a precisely defined cavity with a single micrometer-scale photolithography step[42]. The main steps are illustrated in Fig. 2.9a. First, a cavity is wet etched in dilute hydrofluoric acid to form the undercut region between the SiN mask and the substrate. A thin metal layer is then evaporated at 45° to the substrate. Ion beam milling is subsequently done at -45° to remove a portion of the metal layer in the cavity, which results in a nanoscale hard-etch metal mask layer. This process is simple and applicable to wafer-scale; however, lateral dimensions are difficult to control.

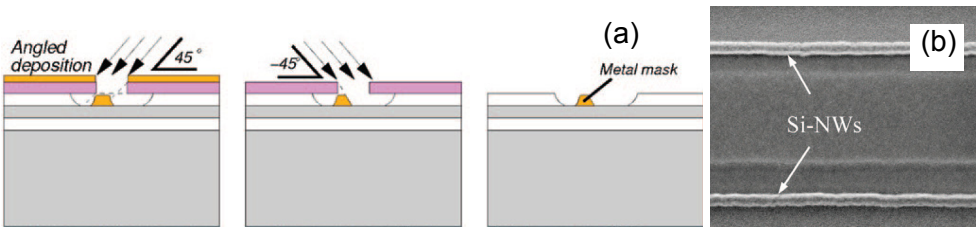

Figure 2.9 (a) Schematic of DEA process (b) SEM images of 100 nm Si-NWs.

e) Lateral anisotropic etching technique

Lateral anisotropic etching technique was used for fabricating Si-NWs as illustrated in Fig. 2.10[62]. With EBL to pattern the surface structures in a nanometer scale, and then wet anisotropic etching as a way to control the crystal oriented features, a minimum top width of 40 nm has been obtained.

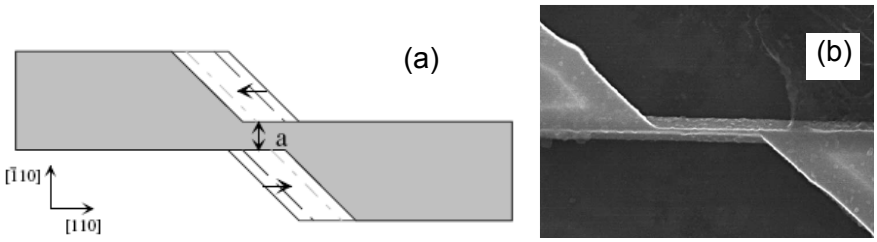

Figure 2.10 (a) Plain view of the mask underetching the tow horizontal arrows indicates the Si edge movement during the etching. (b) A SEM image of the wire.

There are many more techniques for the fabrication of NW structures in literature, and are not introduced here in detail, such as lithographically patterned NW electrodeposition[63], and shadow edge lithography[64]. With most patterning methods, the structures have to be transferred to the device layer either by dry etching or wet etching, both silicon anisotropic etching methods. The most common technique for dry anisotropic etching is reactive ion etching (RIE), which is regarded as a method with high reproducibility and uniformity on wafer scale, and is compatible with semiconductor production technology. It can be used to etch nanostructures with high aspect ratio (> 10)[67]. However, RIE can cause substrate damage and can degrade device performance[43], the rough side walls formed by RIE also results in electron mobility degradation[68]. For wet etching, the etchants used commonly are potassium hydroxide (KOH) and tetra methyl ammonium hydroxide (TMAH). The etchant etches the (100) and (110) planes much faster than (111) plane, thus leaving the mesa structure with atomic smooth (111) sidewalls. Figure 2.11 shows some Si-NW structures fabricated with RIE (Fig. 2.11a, b) and wet etching (Fig. 2.11c, d).

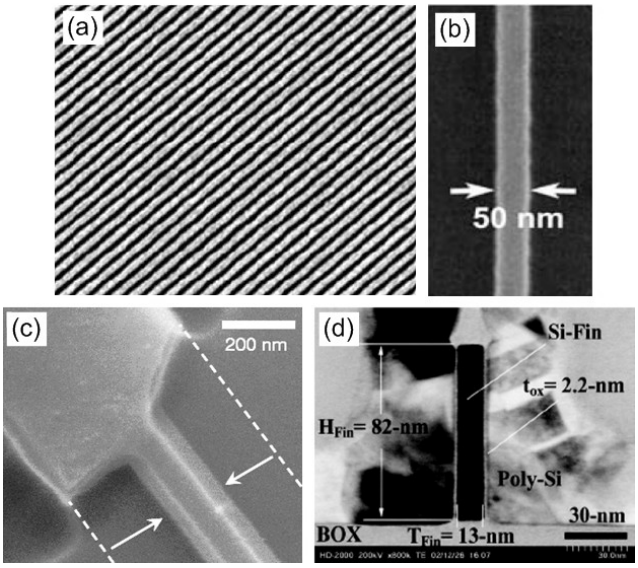

Figure 2.11 Images of Si-NWs fabricated by (a) (b) dry etching, NW arrays with width of 17 nm[65] and a 50 nm single NW[15], and by (c)(d) wet etching on (100)[44] and (110)[66] wafers.

2.4 Biological and chemical applications of Si-NW FET sensors

There has been a large variety of applications featuring Si-NW FET sensors since their first introduction as biosensors in 2001[8]. Devices based on NW FETs are powerful and can be used for ultrasensitive, electrical sensors for the direct detection of biological and chemical species[69]. In this section, applications of Si-NW FET as pH sensor, biosensor and others are broadly reviewed.

2.4.1 pH sensor

The first demonstration of FET device as ion-sensitive FETs (ISFETs) for pH sensing was in 1970s[70], which attracted a lot of attention. With the introduction of Si-NW devices, the pH sensing behavior was originally studied for the purpose of characterizing device properties[8, 10]. The surface potential of NW FET sensor is modulated by the change of pH in the solution, while the gate oxide (e.g. SiO_2, Al_2O_3) undergoes protonation and deprotonation as shown in Fig. 2.12a. Thus the Si-NW pH sensor is gated by the hydrogen ion concentration and the signal can be measured through a conductance change. The pH measurement on a bare SiO_2 surface shows a non-linear response especially at low pH (Fig. 2.12b) and are in

excellent agreement with previous measurements of pH-dependent surface charge density derived from silica[8]. The modification of the SiO_2 surface with 3-aminopropyltrethoxysilane (APTES) provides a surface terminating in both $–NH_2$ and –SiOH groups. At low pH, the $–NH_2$ group is protonated to $–NH_3^+$ and act as a positive gate, which depletes the p-type NW channel and reduces the conductivity. At high pH, –SiOH is deprotonated to $–SiO^–$, which act as negative gate and accumulates p-type channel. A linear relation between the surface potential and pH values of the solution[8], as shown in Fig. 2.12, was observed due to the combined acid and base behavior of both surface groups. The further improvements of pH sensing behavior were achieved by depositing other pH sensitive oxides, e.g. Al_2O_3[71], Ta_2O_5[72]. Knopfmacher et. al.[73] demonstrated this by depositing a thin layer of Al_2O_3 on Si-NW surface by atomic layer deposition. The thin Al_2O_3 layer not only improves the linearity and sensitivity of the pH sensing, but also suppresses the leakage currents through gate oxide sufficiently.

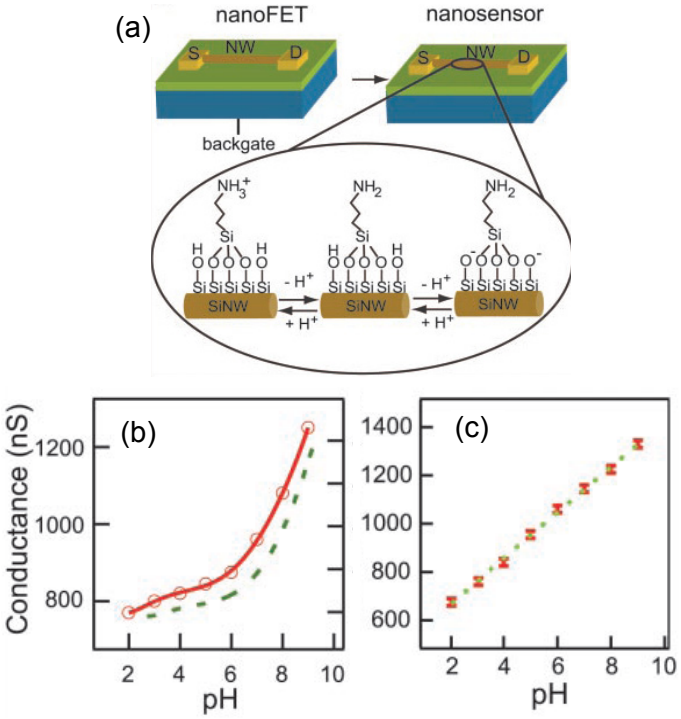

Figure 2.12 (a) Schematic illustration of NW FET for pH detection, and (b)(c) detection of the conductance for a bare and an APTES-modified Si-NW with changing pH respectively[8].

A significant amount of knowledge has been accumulated from conventional ISFET sensors over the past 40 years and should be used to fully understand and optimize the sensing performance of Si-NW sensors. An interesting aspect of the majority of the currently reported measurements in solution is that they lack the use of a reference electrode in the sample electrolyte, thus leaving the solution floating. In another case, a pseudo reference electrode made of Pt that is maintained at zero potential has been used[10]. The importance of using a reference electrode for nanoscale transistors was shown later by current modification through liquid potential controlling and noise elimination[74]. Localized Au/Ti gates are applied to NW sensor, allows field-effect control of the surface charge on the NW either by side (Fig. 2.13a)[75] or floating on top of the NWs[76]. The sensitivity of NW pH sensor can be effectively improved by tuning the gate potential[75], while the highest charge sensitivity (in terms of the normalized conductance change $\Delta G/G$) can be obtained by operating the device in the subthreshold regime (Fig. 2.13b)[77, 78].

Nearly all nanoelectronic device work has been developed on planar substrates. Recently, a three-dimensional (3D), flexible nanoscale FET device was synthesized at the tip of an acute-angle kinked Si-NW[79]. The sensing capabilities of the 3D Si-NW probe was tested by recording the response to variations in solution pH within a polydimethylsiloxane (PDMS) microfluidic channel. Stepwise potential increases from 7.5 to 6.7 by 0.1 pH units were readily resolved, and the sensitivity of ~ 58 mV/pH was obtained to be near the Nernstian limit over a pH range from 7.4 to 7.5.

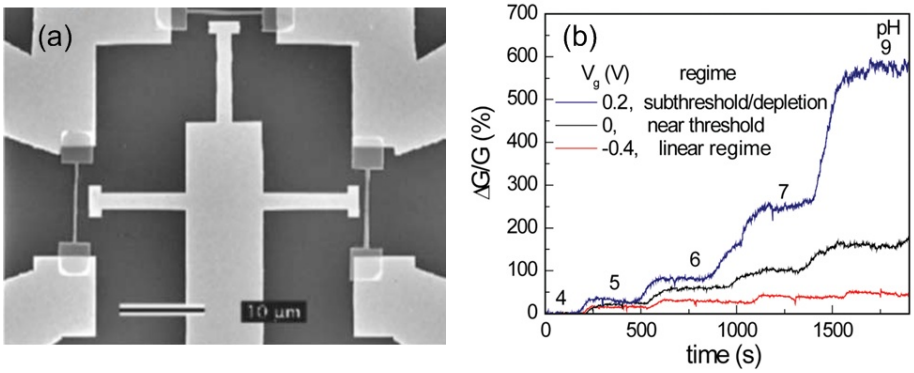

Figure 2.13 (a) SEM image of local gates applied to three Si-NW devices[75], (b) pH measurements at different gate voltages[78].

2.4.2 Biosensor

Si-NW FETs have been demonstrated for high sensitivity measurements of local surface potential changes associated with binding and unbinding of a variety of analysts, such as proteins, nucleic acids, viruses, tissues and cellular bioelectricity/biochemistry from NW surfaces[8-10, 15, 19, 44, 49, 69, 79-98]. Biomolecules that are charged in buffer solution induce surface potential changes when immobilized on NW surface, and thus can gate NW devices and cause conductance changes.

2.4.2.1 Proteins / viruses

The detection of several disease biomarkers have been realized with Si-NW FET biosensors. Cui et al.[8] first reported the use of biotin-modified p-type Si-NW for the detection of streptavidin down to picomolar concentration. Biotin-modified NWs were prepared by depositing a drop of phosphate-buffered solution of biotinamidocaproyl-labeled bovine serum albumin on Si-NWs. A time-dependent increase in the conductance can be resolved immediately after streptavidin addition at very low concentration. As shown in Fig. 2.14, the addition of 250 nM streptavidin solution leads to conductance increase of about 50 nS (3% change). The increase in conductance is consistent with the binding of negatively charged

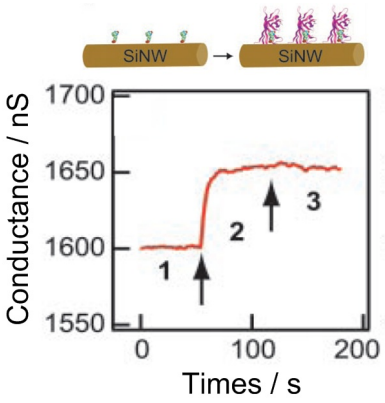

Figure 2.14 Schematic illustration of a biotin-modified Si-NW and subsequent binding of streptavidin (top) and plot of conductance versus time for a biotin-modified Si-NW, where region 1 corresponds to buffer solution, region 2 corresponds to the addition of 250 nM streptavidin, and region 3 corresponds to pure buffer solution (bottom)[8].

streptavidin to the p-type Si-NW surface at the pH of the measurements. The concept of using receptors/ligands modified Si-NW surface for the specific detection has been explored in many directions. Antigen-functionalized Si-NWs show reversible antibody binding and concentration-dependent detection in real time[8]. Specific binding of PSA with the antibody of PSA immobilized on the Si surface through a covalent linkage leads to a conductivity change in response to variations of electrical field at the surface. PSA concentration as low as 1 fg/ml was detected[85]. Besides, the breast cancer biomarker (protein CA 15.3)[99], cardiac biomarker (cardiac troponin-T)[90], vascular endothelial growth factor[91], and the interactions between human estrogen receptors and estrogen-response elements[96] are sensitively detected with Si-NW FET devices.

One advantage of using NW devices for electrical detection is the realization of device integration and electrical addressable multiplexed recording. Simultaneous detection of multiple biomolecular targets is important for medical diagnostics and monitoring the response for better patient treatment[87]. Multiplexed real-time monitoring of protein markers with an array of Si-NW devices allows the rapid detection of many markers with high selectivity and sensitivity. Prostate specific antigen (PSA), PSA-α1-antichymotrypsin, carcinoembryonic antigen and mucin-1 were detected simultaneously with detection limit of 0.9 pg/ml in undiluted serum samples[82]. During the early development of NW biosensors, the real-time label-free detection of a single virus particle by antibody-modified Si-NWs was reported[81]. A two-step procedure was used to covalently link antibody receptors to the surface of the Si-NW. The device was first modified with 3-(trimethoxysilyl)propyl aldehyde, and then coupled with mAb receptors anti-hemagglutinin for influenza A. Figure 12.15 shows the discrete conductance change characteristics of binding and unbinding in the presence of influenza A together with optical measurements using a fluorescence label.

The fundamental limitations to device sensitivity arise from the analyte transport to the very small surface area of NWs[16]. To overcome this limit, dielectrophoresis was applied for protein accumulation to the NW surface. The report shows that NW devices modified with antibody for PSA exhibit up to a 10^4 increase in sensitivity due to streaming dielectrophoresis and corresponding electrostatic contribution to the binding affinity after AC electric-field application[19].

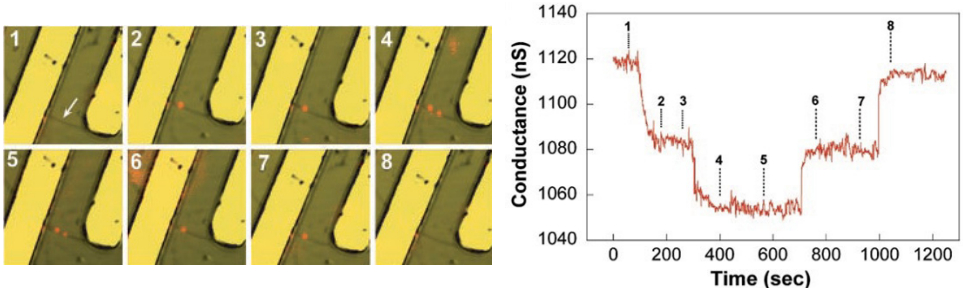

Figure 2.15 Simultaneous conductance and optical vs. time data recorded from a single NW device with a low density of anti-influenza type A antibody[81].

FET sensors normally detect charged species as mentioned above. Special techniques are needed for detecting neutral targets. For a specific case, an uncharged steroid was detected with a Si-NW FET by binding an engineered steroid-binding protein, which was chemically modified with a charged reporter molecule[100]. As shown in Fig. 2.16, in the presence of a steroid, the negatively charged reporter, which presumably occupies the steroid-binding site, is expelled and exposed to the NW surface. The sensitivity of this device can attain a femtomolar level.

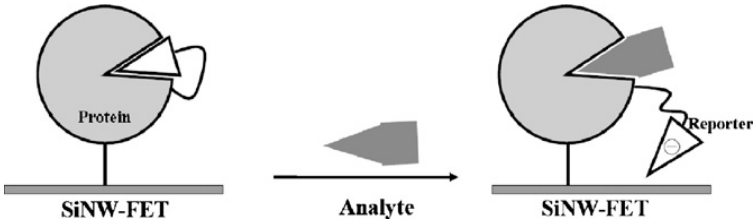

Figure 2.16 Design of a Si-NW FET sensor for detection of an uncharged analyte.

2.4.2.2 DNA detection

Si-NWs for the real-time, label-free detection of DNA and DNA mismatches have been reported by different research groups[15, 49, 80, 93]. DNA biosensing with Si-NW device was reported by Wu et al. to detect sub-femtomolar concentrations, and to distinguish DNA strands with one- and five-base-mismatches from complementary DNA sequences[93]. Hahm et al.[80] showed that Si-NW devices functionalized with peptide nucleic acid (PNA) receptors could distinguish wild type (WT) from the

ΔF508 mutation site in the cystic fibrosis transmembrane receptor gene. PNA is a structural DNA analogue containing an uncharged backbone which has been shown to mimic DNA in forming Watson-Crick complementary duplexes with normal DNA[101]. PNA is uncharged in buffer solution; and compared to DNA duplexes, PNA hybrids have higher thermal stability and can be formed at low ionic strengths. Thus PNA probes can be effectively used for DNA detection. Experiments show that PNA probes offer an efficient surface hybridization in combination with the high specificity of DNA binding[102]. The WT DNA can be effectively and selectively detected with concentrations as low as 10 fM[80]. Gao et al. demonstrated a similar sensitivity with PNA functionalized Si-NW arrays for capturing target DNA[49]. Later, with the same sensing schematic, Zhang et. al. showed 1 fM detection limit of miRNA[94].

The field-effect response of the Si-NW sensor decreases as the DNA moves away from the Si-NW surface[89]. Si-NWs with gate SiO_2 coating have been used in most biosensors since oxide can be easily functionalized with silane-based monolayers for biomolecule binding. However, this oxide coating, depending on the thickness, can limit sensor performance[88]. The Si-NWs without the native oxide exhibit improved solution-gated FET characteristics and significantly enhanced sensitivity to single-stranded DNA detection[10]. As shown in Fig. 2.17, the limit of detection was increased by 2 orders of magnitude. Besides increased sensitivity, binding competition between the NW and the underlying oxide is avoided because of the selective functionalization of the Si-NWs[88].

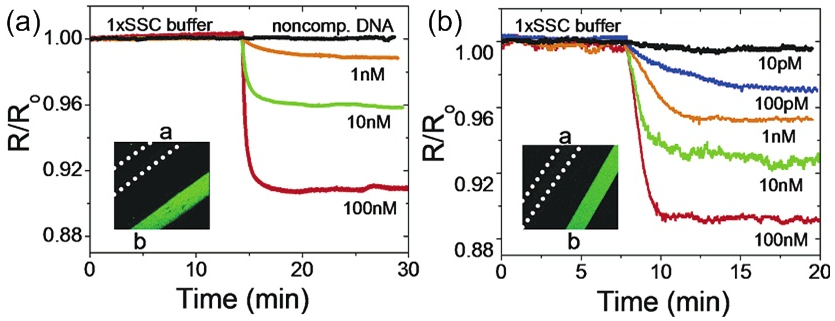

Figure 2.17 Real-time response of Si-NWs for DNA detection with surface functionalization on (a) SiO_2 and (b) Si (without SiO_2)[10].

2.4.2.3 Cellular bioelectricity/biochemical detection

Si-NW FET devices enable noninvasive, high sensitivity, real-time and long-term electrophysiological measurements at the single-cell level or from tissues. Patolsky et al.[83] reported neuronal signal detection, stimulation and inhibition with high-density NW arrays. The Si-NW arrays were patterned with polylysine as an adhesion and growth factor to define neuron cell growth with respect to the device elements. Neurons were then cultured with neurite growth guided along patterned Si-NW arrays (Fig. 2.18a). Figure 2.18b shows the behavior of NW arrays under current stimulation. The correlation between the intracellular and p-type NW trace indicates that depolarization results in negative charging of the extracellular space around the NW. Further experiments were reported using NW transistor arrays for mapping neural circuits in acute brain slices[95]. The small active surface of the NW FET devices provides highly localized multiplexed measurements of neuronal activities with demonstrated sub-millisecond temporal resolution.

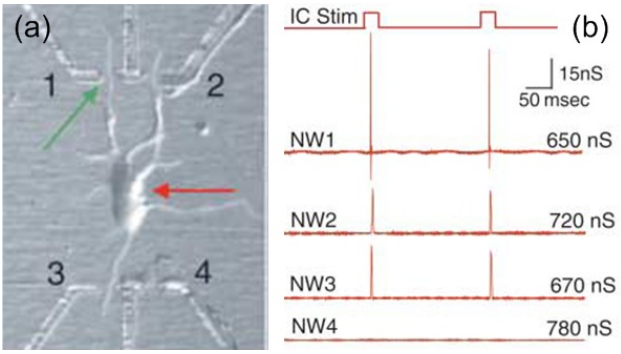

Figure 2.18 (a) Optical image of a cortex neuron connected to three of the four functional Si-NW devices. (b) Trace of intracellular current stimulation and resulting NW electrical response[83].

Electrocardiogram signals recording from beating rat/chicken hearts[92, 98] and spontaneous membrane action potential from individual cardiomyocytes[97] were transduced into a NW conductance change with excellent signal-to-noise ratios. The nanodevices protrude from the plane of the substrate, which can increase NW/cell interface coupling[97]. Hearts or cardiomyocyte cells are placed above the NW surface, and culture for a certain time to get good contact with the NWs (Fig.

2.19a). Figure 2.19b shows simultaneous recording of a chicken heart from a glass microelectrode and Si-NW FET devices. Results illustrate that NW conductance variation is synchronized with the beating heart[98]. Like cardiomyocytes, other muscle cells e.g. rat aortic smooth muscle cells[92] are also electrogenic, thus the membrane electrical activities can be sensed by NW after proper interfacing. The bioelectrical signals detected by NWs differ from the recorded action potentials from intracellular or patch-clamp recordings by transducing the local extracellular voltage at the narrow cleft between the adhering membrane patch and the underneath NW into NW current signals[92]. However, the electrical properties of the adhering membrane may differ from the whole cell behavior due to heterogeneous expression of ion channels.

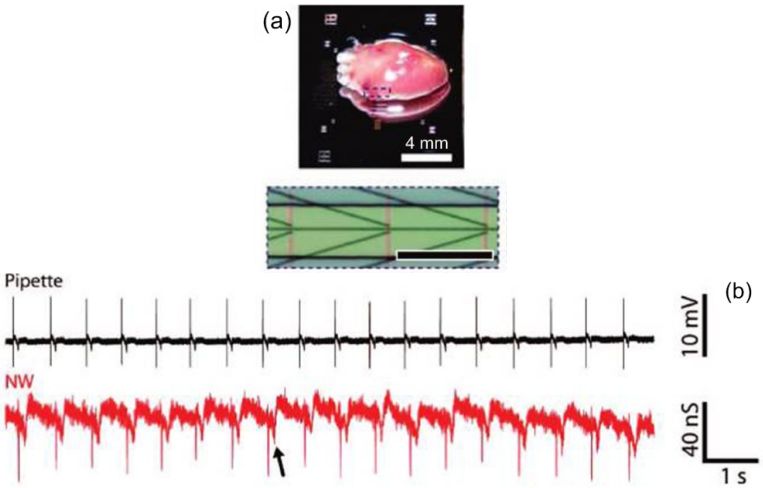

Figure 2.19 (a) Image of heart on surface of a chip. (b) Simultaneous recording from a glass pipette (black trace) and a NW device (red trace)[98].

Besides the detection of bioelectrical signals, biochemical species in liquid are another important aspect to study cell conditions, e.g. under stimulation or drug treatment. The extracellular acidification arising from a small number of T-cells (as few as 200) activated by triggering T-cell antigen receptor was electronically detected by a NW device within seconds after stimulation[103]. Si-NWs for the direct electrical detection of dopamine which is an important neurotransmitter was demonstrated with detection limit in the fM concentration regime[104]. A more

complicated device structure, a microneedle sensor platform with integrated Si-NW tip, was developed for the potential application of intracellular or extracellular biochemical detection[86]. To mimic the transportation of ions and molecules through biological membranes, NWs were coated with a continuous lipid bilayer[105, 106]. A barrier forms between the NW surface and solution species as shown in Fig. 2.20. When the shielded Si-NW transistor incorporates transmembrane peptide pores in the lipid bilayer, it can achieve ionic to electronic signal transduction by using voltage-gated or chemically gated ion transport through the membrane pores[105].

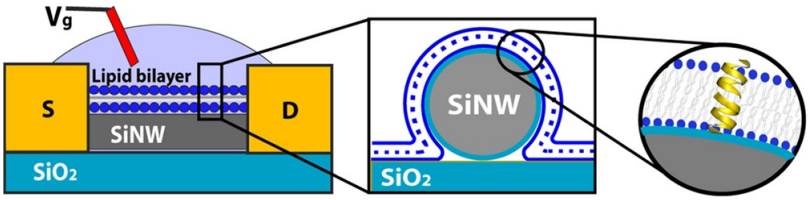

Figure 2.20 Device schematics showing incorporation of lipid bilayer with a NW[105].

2.4.3 Others

Other applications of Si-NW FET sensors include a gas sensor[107], flow velocity sensor[108] and so on. Explosive gases, e.g. (2,4,6-trinitrololuene, TNT)[107] was readily detected at concentration 1 ppb. A Si-NW FET was chemically modified with a monolayer of APTES. TNT molecules can then strongly bind the surface of NW through an acid-base pairing interaction between TNT and amino ligands. Kim et al.[108] reported flow velocity probing with Si-NW sensors. The streaming potential that is generated by the movement of counter ions inside the electrical double layer of the silica substrate induces surface potential change over Si-NW surface. The study highlights the importance of considering the ionic transport in analyzing and optimizing NW FET sensors.

2.5 Conclusion

Recent developments of Si-NW FET sensors are summarized in this chapter. With the progress in Si-NWs research, more efforts were paid to the study of their physical properties, novel fabrication techniques, and various applications. Due to high SVR, Si-NWs show improved sensitivity in detecting biomolecules and have potential applications in even broader field.

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Chapter 3

Fabrication of Silicon Nanowires using Conventional Microfabrication

In this chapter, we report a low-cost top-down Si-NW fabrication technology requiring only conventional microfabrication processes including microlithography, oxidation and wet anisotropic plane-dependent etching. High quality Si-NW arrays can be easily made in any conventional microfabrication facility without nanolithography or expensive equipment. Si-NWs with scalable lateral dimensions ranging from 200 nm down to 10 nm and lengths from 3 μm up to ~100 μm can be precisely formed with near-perfect monocrystalline cross-sections, atomically smooth surfaces. Wafer-scale yields greater than 90% using a novel size reduction method where Si-NWs can be controllably scaled to any dimension and doping concentration independent of large contacting regions from a continuous layer of crystalline silicon. [ii]

[ii] Modified from: S. Chen, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, and A. van den Berg, *ACS Nano* 3, 3485, 2009.

3.1 Introduction

Over the past decade, there has been increasing interest in semiconductor NWs due to their unique electrical, mechanical and optical properties[1-4], especially for label-free biosensing[5-11], however, device and technology development have been limited to a small number of research laboratories typically relying on expensive nanolithography or specialized equipment and processes[11-18]. In general, research over the past five decades has resulted in a large number of nanofabrication techniques and equipment for nanodevice realization with unprecedented precision; largely fueled by the semiconductor industry's need for ultra-high density semiconductor circuits and systems. The Si-NW nanofabrication toolbox consists of techniques that can be broadly classified as either bottom-up or top-down. Bottom-up nanofabrication is in principle simple and provides many high quality materials, however, suitable methods for accurate NW alignment are lacking, and electrical contact formation is problematic, making it difficult to construct functional device arrays[18]. Several key advantages favoring top-down Si-NW nanofabrication include well-established techniques for nanopatterning, semiconductor doping, electrical contact formation and, very importantly, the commercially availability of high quality silicon-on-insulator (SOI) substrates. Conventional top-down nanopatterning techniques, such as deep-UV[9] and immersion deep-UV photolithography are currently the standard for semiconductor manufacturing, however, are extremely expensive and accessible only to large-scale integrated circuit manufacturers. Advanced nanopatterning, such as electron beam lithography and focused-ion-beam lithography can write feature sizes below 10 nm, however, serial patterning is not practical for wafer-scale fabrication and equipment and operation is typically expensive. More recently, Si-NW arrays with 15 nm lateral dimensions have been realized with nanoimprint lithography[14], however, the replication stamp fabrication is complicated and wafer-level patterning remains problematic.

In this chapter, we present a new simple Si-NW fabrication technology that requires only two microlithography steps and conventional microfabrication processes on SOI wafers to form long (ranging from a few microns up to ~100 μm) Si-NWs with scalable lateral dimensions ranging from 200 nm down to 10-20 nm with near-perfect crystalline cross-sections, atomically smooth surfaces and wafer-

scale yields greater than 90% using a novel size reduction method where NWs can be controllably scaled to any dimension and doping concentration, independent of large contacting regions, from a continuous layer of crystalline silicon.

3.2 Top-down Si-NW microfabrication

3.2.1 Fabrication method

The new Si-NW fabrication technology is shown in the brief process sequence of Fig. 3.1. Two types of commercial SOI substrates (p-type DL and handle layer) have been used, including silicon implanted with oxygen (SIMOX, Ibis, Inc., U.S.A.; Si DL: 200 nm, BOX: 150 nm) and UNIBOND (SOITEC, Bernin, France; Si device layer (DL): 200 nm, BOX: 400 nm). The silicon device layer is implanted with BF_2^+ ions (energy: 30 keV, dose: 10^{13} cm^{-2} and angle: 7°). The thermal annealing steps for dopant activation and redistribution are distributed throughout the fabrication process. A thin silicon nitride (SiN) layer is first patterned on the silicon device layer along the [110] direction, which is a mask for the first plane-dependent wet etching (PDE) step. 40 nm of low-stress Si-rich Si_xN_y layer is deposited onto the silicon device layer by low-pressure chemical vapor deposition (LPCVD) at 850 °C. The thin (<100 nm) low-stress Si_xN_y layer is required to prevent the formation of dislocations in the silicon layer due to stress generated by the volume expansion of the silicon dioxide layer during thermal oxidation. The first lithography mask is aligned to the wafer flat, and the Si_xN_y layer patterned and selectively removed with RIE (Fig. 3.1a,b). Lithography alignment errors are less than 1°. The [110] crystalline planes are aligned to the wafer flat within ±0.5°. The exposed silicon is then etched in a dilute tetra methyl ammonium hydroxide (TMAH, 5%, $C_4H_{13}NO$) etching solution. The (100) planes etch 5-10 times faster than the (111) planes in an alkaline etchant, resulting in a trapezoidal silicon region with precisely defined sidewall angles (≈54.7°) (Fig. 3.1c), due to the intersection of the (100) and (111) planes. The exposed (111) facets are then thermally oxidized, which results in a small lateral, or localized, silicon oxidation at the Si/Si_xN_y interface (Fig. 3.1d). The localized oxide layer protects the top edge of the Si-NW from void formation that has been reported for other masking layers[11, 19, 20]. The local oxidation is done in a dry environment (950 °C, 15 min) to form 19nm of SiO_2.

The second lithography step is used to pattern and etch a 50-nm-thick layer of LPCVD polycrystalline silicon (polysilicon), which was deposited at 550 °C. The polysilicon is etched by commercial photoresist developer (e.g. OPD), which has almost no etching to SiO_2 (non-observable after etching for 1 hour), with photoresist as mask for over 1 hour due to the slow etch rate to polysilicon (~ 1 nm/min under yellow light). Practically, during the cooling of wafers after polysilicon deposition, a thin SiO_2 layer will be formed on the surface, which acts as a protection layer during polysilicon etching. The conformal polysilicon etch mask is critical for effectively masking the Si_xN_y etch without damaging the Si-NW surfaces. The Si_xN_y layer is then selectively removed using hot phosphoric acid (85% H_3PO_4, 180 °C) and later the polysilicon layer is removed during the second PDE etching. A second PDE step (TMAH 5%, 60 °C) forms the triangular Si-NWs(Fig. 3.1f), where the base (100) plane is in contact with the buried oxide layer and the (111) planes form the upper surfaces. The Si-NW dimensions can be further reduced as desired using a simple and controllable method for selective size-reduction while the contact regions remain the same thickness as the original silicon device layer, thus integrating macroscale electrical interconnects with nanoscale device regions from a continuous layer of single crystal silicon (Fig. 3.1g).

For applications requiring a gate dielectric, a thin oxide layer (~19 nm) is grown on the Si(111) surfaces, which in all cases results in a rounded tip of the triangular Si-NW. The wafer is then annealed in N_2 atmosphere (950 °C, 20 min) forming a uniform doping concentration, electrically activating the dopants and to minimize the fixed charge in the oxide layer. For electronic devices, two additional lithography steps are required to form electrical contact regions to the Si-NWs and substrate. Prior to the metal contact formation, the removal of the Si_xN_y on the contact pads by RIE and etching of BOX with a buffered hydrofluoric acid (BHF) wet etch are performed. Then a 400-nm layer of Al is deposited on the contact regions and annealed (400 °C, 20 min. and 5% H_2 in N_2) to form good contact between the silicon and the metal layers. It should be noted that for p-type (e.g. B) devices and contact regions, ohmic contacts can be formed with doping levels as low as $\sim 10^{17}$ cm^{-3} when Al and subsequent annealing is used. The low temperature hydrogen anneal also reduces the interface state density D_{it} at the SiO_2/Si interface.

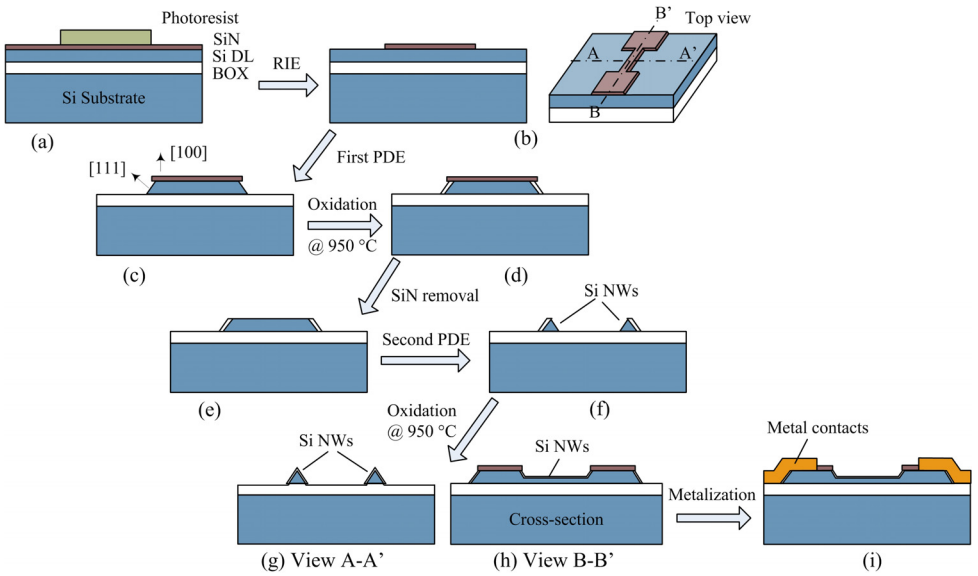

Figure 3.1 Top-down Si-NW microfabrication procedure (not to scale). (a) First lithography step for SiN layer patterning. (BOX: is the buried oxide layer and Si DL: is the silicon device layer of the SOI substrate). (b) SiN layer etching. (c) PDE the DL. (d) Local oxidation step. (e) Removal of the SiN mask layer. (f) Second PDE step and size reduction etching. (g) Gate oxide growth cross-section A-A'. (h) Cross-section B-B'. (i) Contact metalization.

3.2.2 Nanoscale imaging

With sub optical diffraction limit sizes, nanostructures are not observable with conventional optical microscopes, and special imaging methods are required to estimate their dimensions. High resolution scanning electron microscopy (HRSEM, Zeiss 1550) images are obtained at low operating voltages to reduce charging effects on oxidized silicon surfaces. A Digital Instruments Dimension 3100 was used for all atomic force microscopy (AFM) imaging. All AFM images were performed in tapping mode with ultra sharp (average tip diameter ~2 nm) single crystal silicon tips (SSH-NCH-10, NanoandMore, Gmbh). Si-NW transmission electron microscopy (TEM) samples were prepared by depositing a 100 nm thick LPCVD Si_xN_y protection layer onto the upper surface. The sample slices we prepared with a dual-beam focus ion beam (FIB) (FEI Tecnai G2 F20 X-Twin FEG TEM, Maser Engineering, Enschede, The Netherlands) and transferred to a TEM

imaging grid. High-resolution TEM (HRTEM) imaging (FEI 3D-Strata DB-FIB FEG, Maser Engineering, Enschede, The Netherlands) was operated at 200 kV acceleration voltage.

3.3 Results and discussion

Figure 3.2 shows multiscale microscopy images representative of Si-NWs fabricated with this technology. Although the local oxidation method has been previously reported for the fabrication of Si-NWs[21], we present significant new advances including conformal masking, selective size reduction and defect-free ion-implantation impurity doping, and a continuous recessed silicon layer that connects the NWs to microscale electrical contact regions, which facilitates reliable low resistance electrical contacts. Currently, our test dies have about 200 Si-NW devices (Fig. 3.2a), however, this fabrication technology is capable of producing high-density Si-NW arrays with device diameters down to 10-20 nm and pitches ~50-60 nm with the use of high resolution patterning methods to define the initial Si_xN_y masking layer (Figs. 3.1a). However, the majority of applications do not require ultra-high density device arrays. The multiscale microscopy images clearly demonstrate the remarkable effectiveness of this fabrication technology for manufacturing high quality functional Si-NW devices and arrays with well-controlled sub-30 nm lateral dimensions, smooth (111) surfaces, and high wafer-level yield using only conventional microfabrication processes.

The combination of three key fabrication steps facilitates this new Si-NW fabrication technology, including PDE, localized silicon oxidation, and size reduction etching, and resulting in the new size-reduced recessed Si-NWs. Details of these key process steps are described below in more detail.

3.3.1 Plane dependent etching

Crystal plane dependent processes on silicon surfaces have been known for more than 50 years[22] and have profound effects on the behavior of reactive processes, such as PDE[23-25]. The different crystal planes etch anisotropically by hydroxide ions in alkaline solutions where (111) planes have one dangling bond per unit cell and have the lowest etch rate and the (100) and (110) planes both have two dangling bonds per unit cell and have higher etch rates[25]. Using this technique, we have been able to pattern Si-NWs with lengths up to 100 μm resulting in ratios of

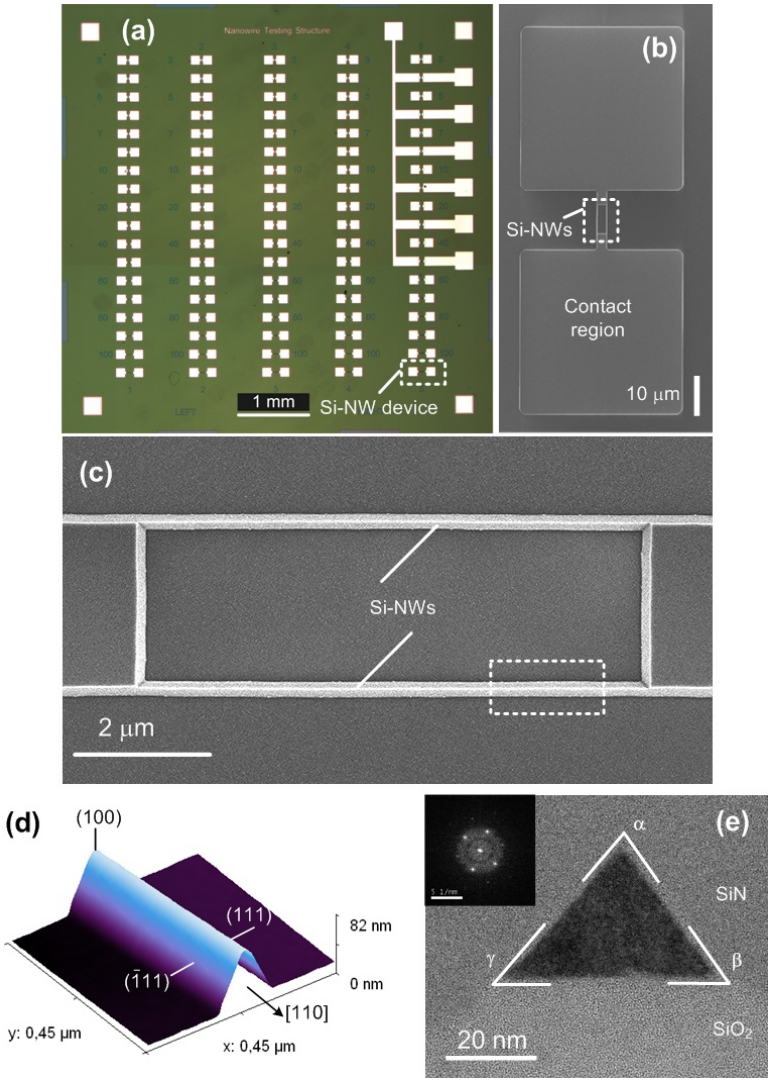

Figure 3.2 Multi-scale microscopy images of fabricated Si-NWs. (a) Optical microscopy image of a die (bright regions are aluminum contact metal). (b) HRSEM image showing electrical contact pad regions and two centrally located Si-NWs indicated with dashed white rectangle (c) HRSEM of triangular Si-NWs (d) Tapping-mode AFM image of single Si-NW (NW height: 60 nm) (e) HRTEM image of monocrystalline Si-NW cross-section with angles α=77°, β=54.7°, and γ=48°. Inset: diffraction pattern indicates [011] zone axis along the device length.

the lateral dimensions to length dimensions of more than 10^4.

The wide application of PDE has been facilitated by the availability of high-quality silicon wafers with low defect densities, low thickness variations and precise control of crystal plane alignment with wafer flats. Figure 3.3a shows a silicon unit cell for selected planes, and Figure 3.3b shows wafer flat alignment with the crystal planes of a (100) silicon wafer, where horizontal and vertical gray lines indicate the [110] directions which are aligned to the edges of Si_xN_y layer (Fig. 3.1b). The alignment tolerance is ±0.5º [26]. This arrangement is compatible with conventional micro-lithography alignment systems where the wafer flats can be precisely aligned to features on the photolithography mask plates. Nearly atomically smooth (111) surfaces were obtained after PDE etching. This provides another advantage of this fabrication technique, the (111) silicon planes are ideally suited for direct organic monolayer formation, which is important for biological interfacing applications, such as biosensing.

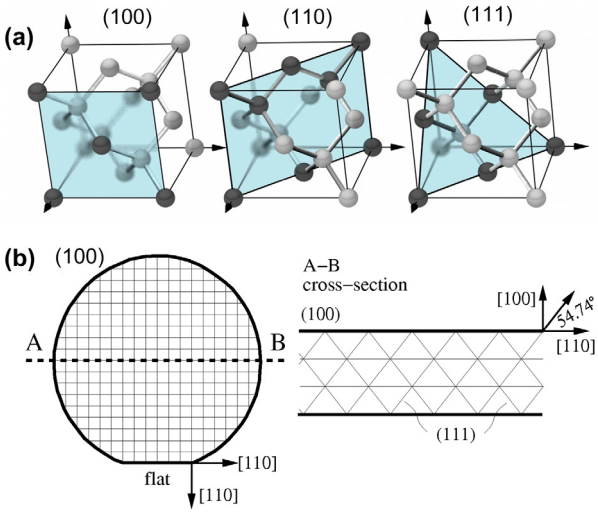

Figure 3.3 (a) Silicon unit cell for selected planes, (b) Crystal plane alignment with wafer flat for commercially available (100) silicon wafers and corresponding wafer cross-section.

A correlation was found between the etch rates and their activation energies with slowly etching crystal surfaces exhibiting higher activations compared to fast etching surfaces with lower activation energies[25, 27]. An electrochemical model was proposed to explain the plane dependent etching behavior due to small differences

in the energy levels of the back-bond surface states as functions of crystal orientation[25]. This indicates that two silicon back-bonds must be broken to etch the (100) and (110) surfaces and three for the (111) surface. Based on this, Seidel *et al.* reported that the activation energy of an Arrhenius relationship $R \sim R_o e^{-E/kT}$ follows $E_{(110)} < E_{(100)} < E_{(111)}$, which correlates with the measured etch rates for alkaline etching solutions. Typical PDE ratios for potassium hydroxide (KOH) at room temperature are $R_{(110)} / R_{(111)} \sim 160$ and $R_{(100)} / R_{(111)} \sim 100$[25], and for tetra methyl ammonium hydroxide (TMAH) at 60 °C are $R_{(110)} / R_{(111)} \sim 40$ and $R_{(100)} / R_{(111)} \sim 20$[27, 28].

3.3.2 Local silicon oxidation

The local oxidation of the Si/Si_xN_y interface at the edge of the (111) surface and the (100) plane is used to prevent etching of the upper (100) plane. Figure 3.4a illustrates the details of LOCOS. The local oxidation of silicon at the Si/Si_xN_y interface has been well studied[29] and the lateral oxidation in the *x*-direction (Fig. 3.4) provides a uniform oxide protection layer along the *z*-direction on the silicon surface that facilitates the formation of Si-NWs with large aspect ratios (> 10^4). The local oxidation results from the lateral diffusion of oxidant and subsequent

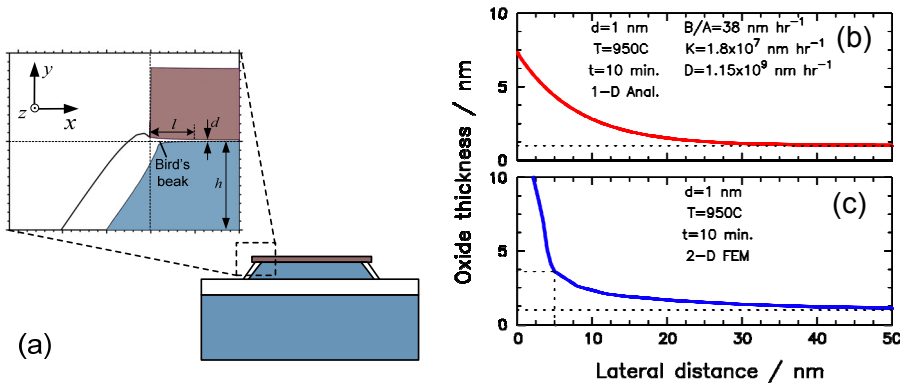

Figure 3.4 (a) The local oxidation of silicon forms a protective region at the corner regions of the silicon mesa structure, allowing the precise formation of Si-NWs with arbitrary dimensions. Enlargement: graphical results of a two-dimensional finite element simulation (blue:Si; white:SiO_2; brown: Si_xN_y). The local oxidation of silicon (b) Analytical model for dry oxidation and d = 1 nm behavior (c) 2D FEM with d = 1 nm.

reaction with the silicon, which produces a volumetric expansion of the SiO_2 interface layer that vertically displaces the Si_xN_y masking layer and produces the well known "bird's beak" effect shown in Fig. 3.4, which is the result of a two-dimensional finite-element numerical simulation (Taurus TSuprem-4, Synopsis).

The lateral oxidation distance l is strongly dependent on the initial oxide thickness between the SiN and silicon device layer d[29]. The oxidation rate as a function of lateral distance and buffer oxide thickness can be approximated by $R_d \approx B/A\, e^{-\sqrt{K/Dd}y}$, where B/A is the linear oxidation constant. Using values of B/A, K and D from[29], the oxide growth has been estimated for d = 1, shown in Fig. 3.4a. The final oxide thickness is strongly dependent on d. For d = 1 nm, the lateral oxide growth extends $l \sim 20$ nm and extends $l \sim 30$ nm for d = 3 nm. The horizontal dashed line indicates the initial thickness of the buffer oxide layer. Although this simple model predicts an increased final oxide thickness, it has been shown that for no buffer oxide layer (d = 0) very little lateral oxidation occurs[29]. Since this simple model assumes a continuous (100) silicon surface, a two-dimensional finite element numerical model (TSUPREM-4, Synopsis, Inc.) of the lateral oxidation distance including viscoelastic oxide flow in the y-direction has been performed. The movement of the oxide/silicon interface is two-dimensional (perpendicular to the interface), and variation of crystal orientation along the interface is taken into account when calculating the oxidation rate. The viscoelastic oxide flow is calculated in two dimensions by using three-node finite element numerical model that allows stress to be estimated (Fig. 3.4)[30]. A thin low-stress Si_xN_y layer should be used to reduce the risk of the dislocation formation[29, 31].

3.3.3 Size reduction

The most common top-down Si-NW fabrication approach is to first reduce the silicon device layer thickness, followed by nanopatterning and subsequent pattern transfer to form the Si-NW. However, thin electrical contact regions for very thin DL can lead to high contact resistances[18] and conventional doping methods can be difficult to control. A self-limiting dry oxidation and subsequent selective removal of the oxide layer has been reported[9, 12, 32], however, resulted in non-uniform oxidation rates due to stress concentration located at shape transitions or sharp points, as well as losing of dopant atoms during the oxidation step. Electrochemical

size reduction etching can be operated in low temperature, and NW sizes down to 10 nm can be routinely generated from initial size of 100-200 nm[33, 34]. However, each NW needs electrical contacts during the etching, and the fabricated structure are subjected to high non-uniformity.

A simple and controllable method is presented for the selective Si-NW size-reduction of dimensions down to ~10-20 nm while maintaining thick contact regions in a continuous layer of single crystal silicon. Using the silicon dioxide from the initial local silicon oxidation step (Fig. 3.1d) as a protection layer, the exposed (111) silicon planes continue to etch in a controllable way. Figure 3.5 shows measurements of the size reduction etching behavior. The inset plot shows that the etch rate varies from about 29 nm min^{-1} for a 2 minute etch to about 19 nm min^{-1} for a 7 minute etch. All etching data was recorded for 5% TMAH etching solutions at 60 °C. The oxidized surface of the Si-NW prevents etching of the (100) planes, because all dangling silicon bonds have been terminated with oxygen from the thermal oxidation step (Fig. 3.6a) and only non-oxidized dangling silicon bonds react with the hydroxide ions. The exact number of atoms at the apex of the size-reduced Si-NWs is not known, however, HRTEM images of size reduced Si-NWs show a relatively sharp transition at the intersection of the (111) and ($\bar{1}11$) planes (Fig. 3.6a). The Si-NW width can be precisely determined from height measurements (with TMAFM) using $w \approx 2h$ / tan(54.7°). Figure 3.7a-c shows various dimensions of Si-NW structure with both AFM images and HRSEM images, from height of 135 nm down to 20 nm. The size-reduction etch process can be further improved by reducing the etch process temperature, which will improve the control of the final device dimensions. A key advantage of this new size reduction method is that the electrical contact regions are not reduced in thickness, thus providing reliable low-resistance contacts, and the Si-NW device regions are recessed to the desired dimensions in a thin silicon region (Fig. 3.6b).

High-resolution TEM cross-sections (Fig. 3.7d) of two representative Si-NWs show monocrystalline silicon and the accompanying diffraction patterns (Fig. 3.2e, inset) indicate that the [011] crystal direction lies along the device length as expected. The measured intersectionangles between the (111) and (100) planes are $\alpha \approx 77^{\circ}$, $\beta \approx 54.7^{\circ}$ and $\gamma \approx 48^{\circ}$. Ideally, we expect $\alpha = 70.6^{\circ}$ and $\beta = \gamma = 54.7^{\circ}$ and the small deviation is due to the slight curvature of the left arm of the triangular

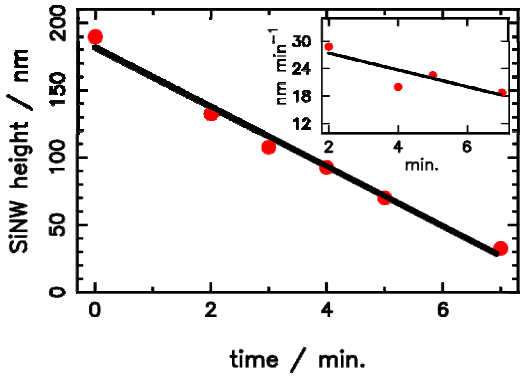

Figure 3.5 Measured Si-NW size reduction as a function of etch time (each data point represents an average of 5 measurements), Inset: shows the variation of etch rate with time.

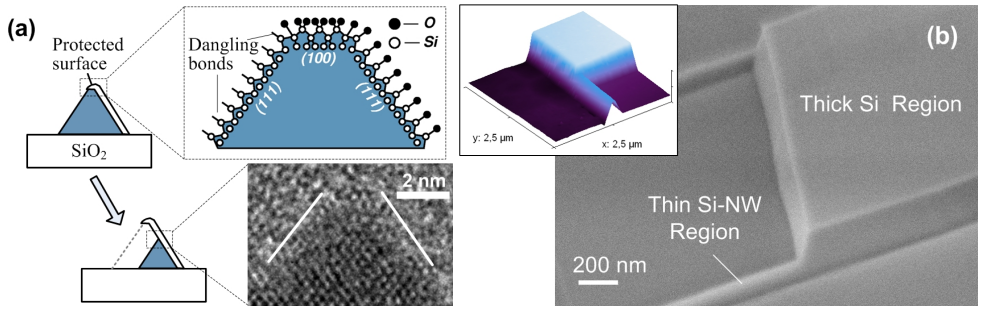

Figure 3.6 (a) Size reduction etching scheme. Upper right: Ideal atomic structure of the Si(111)/SiO_2 and Si(100)/SiO_2 interfaces (not to scale). Lower right: HRTEM of size reduced Si-NW apex. (b) HRSEM image of size reduced recessed Si-NWs showing interface between microscale electrical contact region and size reduced Si-NW from a continuous layer of silicon, Inset: TMAFM image.

structure caused by the initial oxidation of the (111) surface, which has a non-uniform growth rate near the sharp edges. These crystal plane inconsistencies are more pronounced as the Si-NW cross-section is made small (h~25 nm in this case), and we have measured intersection angle deviations ~1-2° for structures with h~100 nm. Additionally, reducing the thickness of the thermal oxide or using in combination with a non-reactive oxide deposition can reduce the curvature of the (111) surface.

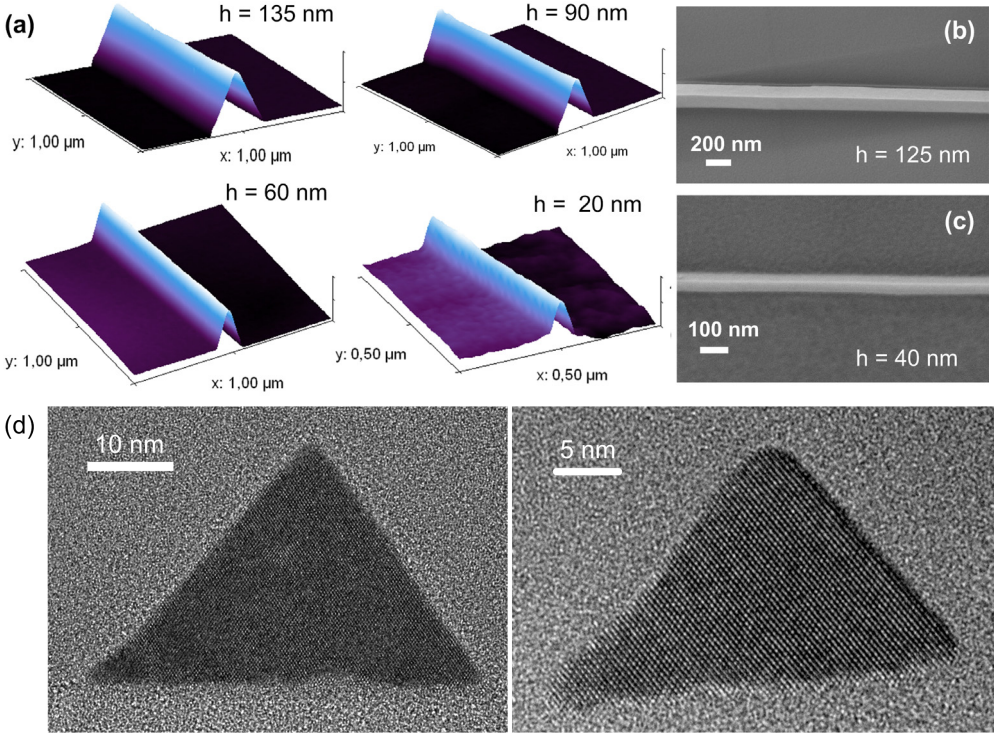

Figure 3.7 Size reduced recessed Si-NWs. (a) TMAFM images with different dimensions. (b) and (c) HRSEM images. (d) HRTEM image with h = 25 nm and 15 nm.

3.4 Conclusion

In summary, a new scalable Si-NW fabrication technology has been developed, based on a combination of conventional microfabrication steps that does not require expensive nanolithography to form sub-30 nm feature sizes. The advantage of this technology is that moderately dense arrays of Si-NWs, with precisely controlled dimensions and atomically smooth surfaces, are directly and simultaneously fabricated with thick microscale electrical contact regions from a continuous layer of single crystal silicon using a novel size reduction method. Si-NW device arrays with lateral dimensions down to 10-20 nm and lengths up to 100 µm can be consistently fabricated with high wafer-level yields. Our simple Si-NW fabrication technology can be manufactured in any conventional microfabrication cleanroom.

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Chapter 4

Advanced Fabrication Techniques

Advanced fabrication techniques including impurity doping, ohmic electrical contact formation and the effect of channel depletion by Si/SiO_2 formation are all important aspects in Si-NW device fabrication and are discussed in this chapter. The impurity dopant distributions are measured with secondary ion mass spectrometry measurements (SIMS) and estimated with two dimensional finite-element process simulation. The results show the importance of proper doping and annealing processes in order to have well-defined doping profile. Then electrical characterization of contacts and Si-NW device are given to show how they are affected by the fabrication techniques. The contact resistance is ~ 4.4 kΩ/contact, which contributes to less than 1% of the total electrical resistance. The charges and states introduced by Si/SiO_2 formation cause a huge effect to the *IV* characteristics due to the large SVR of Si-NW structure. [iii]

[iii] Modified from S. Chen, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, and A. van den Berg, *ACS Nano* 3, 3485-3492, 2009 and H.D. Tong, S. Chen, W.G. van der Wiel, E.T. Carlen, and A. van den Berg, *Nano Lett.* 9, 1015-1022, 2009.

4.1 Introduction

In chapter 3, we described an easy and robust way to fabricate Si-NW structures using conventional microfabrication techniques. However, the fabrication of a functional NW device requires more than micromachining processes. In this chapter, we will focus on the advanced fabrication techniques for Si-NW devices, including impurity doping, ohmic electrical contact formation and the effect of channel depletion by Si/SiO_2 formation followed by electrical characterization. Since we are developing depletion-mode Si-NW devices, impurity doping is an essential aspect of device design.

4.2 Si-NW impurity doping

4.2.1 Doping basics

Semiconductor materials need to be doped either with p-type (e.g. boron) or n-type (e.g. arsenic and phosphorous) materials in order to be electrically conducting. Si-NWs that are fabricated in top-down are normally fabricated on silicon-on-insulator (SOI) wafers and thus have very thin Si device layer (DL). Special requirements related with such thin layers will be discussed in section 3.2.2. The dopant profile, which strongly influences the electrical characteristics, is generally determined in two steps, the introduction of dopant atoms and subsequent thermal steps. Each dopant type requires a minimum temperature ~ 900 °C for dopant electrical activation. Dopant atoms can be placed on or near the surface of the wafer by ion implantation, gaseous deposition, or by coating the wafer with a layer containing the desired dopant impurity[1, 2]. This step is followed by a drive-in diffusion that transports the dopant atoms into the wafer. The diffusion depth depends mainly on the temperature and the time of the diffusion. Ion implantation as a standard doping method in IC technology is used to introduce dopant ions into the surface layer of silicon. The doping dose, doping energy and angle, together with thermal steps all influence the final doping profile, and are simulated during the designing of fabrication process as discussed later.

4.2.2 Selective ion implantation

Ion implantation is the standard technique for top-down semiconductor manufacturing, with the ability to control the number of implanted dopant atoms precisely[3]. For thin films, shallow implantation is needed to reduce the projected range R_p. There are generally three ways to realize shallow implantation: 1) simply by reducing the implanting energy, which can be down to 5 keV or even lower, 2) using heavy ions, e.g. BF_2 implantation instead of B, results in shallower profiles giving the same implant conditions (energy and ion beam current)[4], and 3) in case of higher implantation energy, to grow a stopping layer, e.g. 20 nm SiO_2 or Si_3N_4, on the Si surface can be used. This stopping layer not only decreases the implantation depth but also reduces the damage of Si surface by high energy ions. However, the disadvantage is that a significant amount of surface layer atoms are also recoil implanted into the Si.

For single crystal silicon, the channeling effect turns out to be difficult to control and leads to anomalous profile tails[3]. The most widely adopted procedure to minimize channeling is to tilt the wafer surface relative to the incident beam direction, most commonly by roughly 7°, so that the lattice presents a dense orientation to the incident beam. Other methods to further reduce channeling includes: pre-amorpholizing the lattice by a prior implantation, implanting through a surface oxide to randomize the directions of the ions and using heavy ions for the implantation. With either tilted at 7° or adding a surface oxide, the projected range parameter for amorphous implantation can be used[1].

In our fabrication process, the Si-NW channel conductivity is selectively controlled using conventional shallow ion-implantation to eliminate implant-induced crystal damage. Figure 4.1 shows secondary ion mass spectrometry (SIMS) measurements of post-implant (a) and post-anneal (b) boron distribution in a 190 nm thick silicon device layer, doped with BF_2 ions at energy of 30 keV, dose of 5×10^{14} cm^{-2} and tilted at 7°. The boron concentration distribution gives the $R_p \approx$ 27 nm, and $\Delta R_p \approx 13$ nm when fit the data with Gaussian distribution function. This means that any crystal damage caused by the implantation is contained primarily in the first 40 nm of the Si DL. Thus following size reduction, the implant region is removed, therefore, our size reduction etching procedure selectively dopes the Si-NW separated from the implantation region. Subsequent thermal annealing at

950 °C (7 min.) results in the redistribution of the dopants and electrical activation throughout the entire thickness of the Si DL as shown in Fig 4.1b. Alternative Si-NW doping methods have been reported, such as spin-on-glass, to eliminate any implant induced crystal defects[5]. In our approach, we benefit from the precise control of doping concentration that ion-implantation provides without concern for damage to silicon device region.

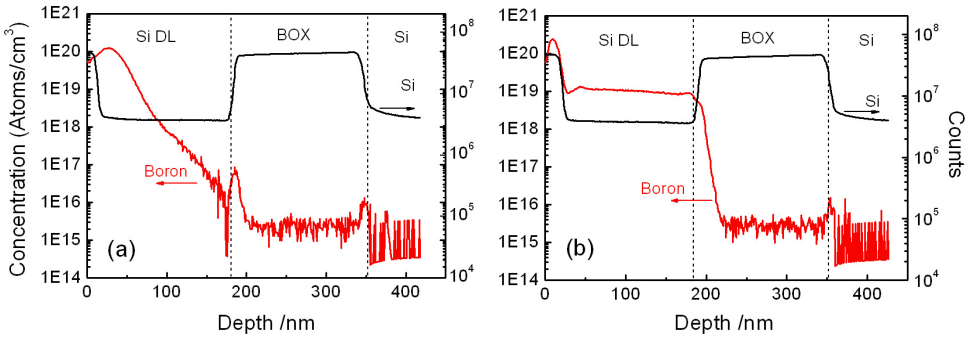

Figure 4.1 Secondary ion mass spectrometry measurements of BF_2^+ ion implantation (energy = 30 keV, dose: 5×10^{14} cm^{-2} and wafer angle: 7°) into a 190 nm thick silicon device layer (a) post implantation B distribution (green trace) (b) post-anneal B distribution (green trace). The background doping concentration of the as-received SOI wafers (SIMOX) ~10^{15} cm^{-3}.

4.2.3 Process simulation

The doping profile of the Si-NW devices can be obtained by simulation with two-dimensional (2D) or three-dimensional (3D) finite element process simulator (Sprocess, Synopsis TCAD). After dopants are introduced into the device layer, they diffuse and redistribute through the structure after the various thermal annealing cycles, which can be modeled using Sprocess. The ion implantation process is computed with the Monte Carlo simulator (Sentaurus MC, Synopsys TCAD) which uses a statistical approach to calculate the penetration of implanted ions into the target and accumulation of crystal damage based on the binary collision approximation[6]. The diffuse model we used is the ChargedReact model, which is the most accurate transport model and the most general model in Sprocess[6].

Figure 4.2a shows the simulated 2D structure cross-section along the length of the NW, with Si DL 200 nm, BOX 200 nm, Si-NW height 140 nm and front oxide (FOX) 15 nm. The implanted ions are BF_2 ions, with implantation energy of 30 keV and wafer angle of 7º the same parameters as used for the real fabrication. The simulated result post-implant is $R_p \approx 25$ nm, similar with the measured value with SIMS. The color in the Si region indicates the doping concentration as indicated in the color bar. The profile was obtained with dose of 10^{13} cm^{-2}, and three thermal cycles as mentioned in Chapter 3 from the real process: 850 °C for 10 min, 950 °C for 15 min, another 950 °C for 35 min (including 15 min oxidization and 20 min of nitrogen annealing). Since boron ions can easily segregate from the thin Si layer (segregation coefficient less than unity), especially tends to accumulate within Si/SiO_2 interface, there will always be less boron dopants in Si after each thermal step. Thus, careful device design and fabrication is crucial in order to have a well-defined dopant concentration and distribution.

Figure 4.2b illustrates the doping profile at two different locations x_1 the contact region and x_2 the Si-NW region as marked in Fig. 4.2a. The doping concentration in the contact region ($x_1 = 0.2$ μm) resemble a Gaussian distribution, with a peak concentration of 10^{18} cm^{-3} near the Si/Si_xN_y interface, which allows ohmic contact (with an annealed Al contact) formation with higher boron concentration over this region. The boron concentration is much less and more uniformly distributed over the recessed Si-NW region ($x_2 = 1.0$ μm), around 10^{17} cm^{-3}, and can be increased with 1) longer annealing time before size reduction to push down the dopants while using the same dose, 2) increase the implantation energy to have a deeper implant depth, or 3) increase the dose. We benefit from the fabrication technique that with a single implantation step, a well-shaped dopant distribution (higher over contact region than NW region) can be obtained. Then both profiles give a sharp increase in the BOX/Si interface due to the segregation of boron into SiO_2 after thermal steps.

Figure 4.2c shows the boron distribution over the width cross-section of Si-NW with the same doping, etching and annealing conditions as mentioned for Fig. 4.2a. However, compared with the 2D length cross-section simulation while NW has only 1D structural confinement (height), NW with 2D structural confinement (height and width) is substantially affected by thermal processes and results in doping concentration of $\sim 1.5 \times 10^{16}$ cm^{-3}. The final oxidation step results in oxidation

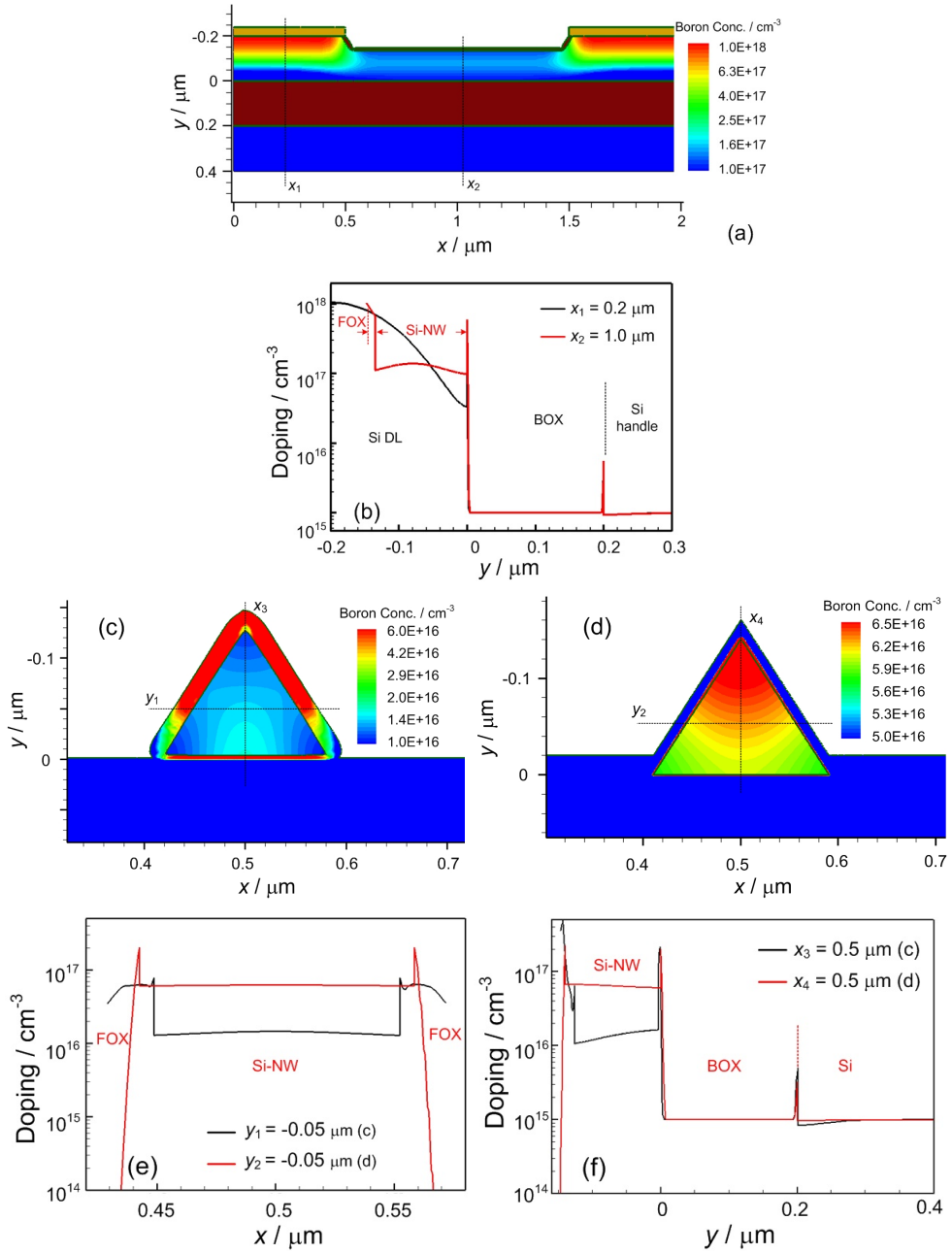

Figure 4.2 (a) 2D simulation of recessed structure, and (b) doping profiles at x_1, x_2, (c, d) simulated structure on width cross-section with high-temperature gate oxidation and low-temperature oxide deposition respectively, (e, f) doping profiles long x and y from (c) and (d). (Boron Conc. stands for Boron concentration).

enhanced diffusion (OED)[7], and can be observed by the lose of dopant atoms in the Si-NW and increased boron concentration in FOX, as shown in Figs. 4.2c, e. A large doping concentration over FOX results in potential leakage with high V_{fg} bias as observed while measured with metal front-gate. This OED effect can be avoided by depositing a thin layer FOX, e.g. atomic layer deposition, instead of oxidation step, a uniform doping concentration of ~6×10^{16} cm^{-3} can be achieved with the same dose and energy, and eventually annealed at 1050 °C for 20 min as the last thermal step instead of at 950 °C to achieve uniform doping. The structure and doping profiles are shown in Figs. 4.2 d, f.

4.3 Electrical contact characterization

4.3.1 Ohmic contact

Contact resistance R_c between the interconnect metal and the silicon layer is one of the important properties for NW electronic device for integrated circuits and sensor systems. It is well known that the formation of ohmic contacts with low contact resistance is crucial for scaling integrated circuits to smaller dimensions with higher packing densities[8, 9]. An ohmic contact is defined as a metal-semiconductor (MS) contact that has a negligible contact resistance relative to the bulk or spreading resistance of the semiconductor and has a linear *I-V* characteristics or negligible effects from the Schottky behavior[10]. The electrical contact should not adversely affect the device performance and supply the required current with negligible voltage drops across the contact structure. There are two basic types of ohmic contacts that depend on the doping of semiconductor region of the contact. For lower doping concentration $N_a \leq 10^{17}$ cm^{-3}, the thermionic-emission current dominates the current transport, and low barrier height should be used to obtain small R_c. For contacts with higher doping $N_a \geq 10^{19}$ cm^{-3}, R_c is dominated by quantum mechamical tunneling process and decreases rapidly with increased doping. The MS contacts can be made ohmic if the effect of the barrier on carrier flow can be made negligible or very thin by high impurity doping levels.

In the case of Si-NWs, significant progress in fabrication technology, using both top-down and bottom-up manufacturing techniques, has been demonstrated in the past several years. However, significant problems still exist in the formation of functional, low resistance contacts. As the dimensions are scaled to the range of 20

nm to 100 nm, the formation of good contacts becomes essential for maximizing performance. The high contact resistance of semiconductor NW devices has been attributed to the small contact area, when compared with conventional FET devices, as R_c is inversely proportional to contact area[11-13] as $R_c = \rho_c/A_c$, where ρ_c is the specific contact resistance, A_c is the contact area, especially when the contact area is small as is the case for most bottom-up Si-NWs. The formation of a large source and drain regions, by forming contacts to relatively large Si pads rather than to the NWs themselves, reliable contacts can be achieved[14].

Planar contact formation has been extensively studied and optimized using conventional MOSFET fabrication technology, and requires consideration of the Schottky barrier and surface contamination. A practical solution to reduce the potential barrier height of the metal-silicon is to properly choose a metal layer with a low work function difference and doping of the region under the contact, such that carrier transport across the MS interface is dominated by quantum-mechanical tunneling and the barrier width is as narrow as possible. Surface contamination, such as residual oxide or polymer layers, is an important issue and can be minimized with large contacting areas and proper cleaning procedures[3].

4.3.2 Contact resistance measurement

For top-down fabricated Si NWs, a planar contact structure is most common, as shown in Fig. 4.3. The contact region can be divided in three main sections: contact metal, high ohmic interface layer and semiconductor with concentration gradient of diffused impurity atoms or thin silicide layer[15]. Interface layers are usually characterized by the specific contact resistance $\rho_c = v_c / j_c$, where v_c is the voltage across the layer and j_c the current density through the layer. The resistance of the Si NW is $R_{NW} = R_s(l/w)$ (Ω), where R_s is the sheet resistance (Ω/sq.) and l and w are the length and width, respectively. The contact metal and the diffused layer are typically a few orders of magnitude smaller than R_s, therefore considered negligible. Thus the total resistance of a NW device can be expressed as a lumped model from Fig. 4.3:

$$R_T = R_{NW} + 2R_c \approx R_s \frac{l}{w} + 2\frac{\rho_c}{\lambda w} \tag{4.1}$$

where $\lambda = \sqrt{\rho_c / R_s}$ is the transfer length, a characteristic distance of the current penetration under the contact layer. Here we assume the contact is much longer than the transfer length.

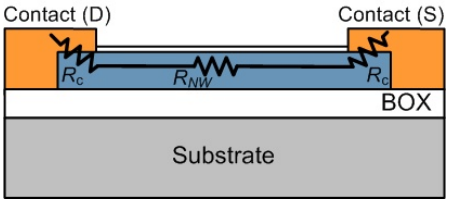

Figure 4.3 NW device with three resistor lumped model.

The standard technique for measuring the metal-semiconductor junction contact resistance is called transfer length method (TLM) when more than three contacts is used, which only requires simple *I-V* curves measurements at a probe station and using a semiconductor parameter analyzer.

The TLM allows the measurement of contact resistance, specific contact resistance and NW resistivity. Different TLM test structures have been developed for NWs, multi-wire structure, multi-contact structure[16-18]. In our case, we use multi-wire structure for device parameter extraction, as shown in Fig. 4.4a of NW devices with varying lengths. Although there have been many methods proposed for estimating the specific contact resistance, this method is simple and convenient provided that the Si-NW dimensions and doping concentration are constant among different devices, which is a reasonable assumption for the top-down fabricated Si-NWs presented here. In this case, as long as $L > \lambda$ the requirement to have all contacts the exact same length is not important. Since the total resistance of the device is modeled as shown in Eq. 4.1, then R_T for each device length l_i ($R_T = f(l)$) can be plotted as shown in Fig. 4.4b. The NW length (l) is plotted on the abscissa and total resistance on the ordinate. From the measured data, a linear fit to the data extrapolated to $l = 0$, which gives an estimate of the contact resistance $(R_T)_{l=0} = 2R_c$, from Eq. 4.1. For the other axis crossing $R_T = 0$, then $(l)_{R_T=0} = -2\lambda$. The slope of the linear expression is then $\rho_s/A_s = R_s/w$. More detailed modeling of the contact structure is required to understand the current distribution in the widened contact

structures. Figure 4.4b shows the relevant parameters extracted from a linear fit to the data measured from devices shown in Fig. 4.4a. Now the multiple length Si NW structures can be measured using 2-probe measurements to estimate the specific contact resistivity, penetration length and sheet resistance of the silicon layer.

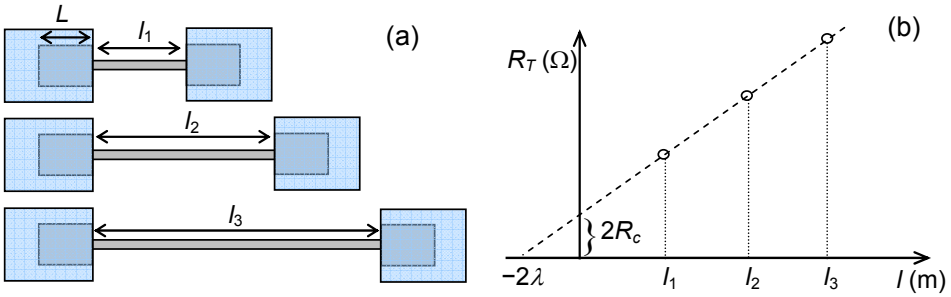

Figure 4.4 (a) Multiple NW with varying lengths used to extract the contact resistance (b) Example of the R_T plotted as a function NW length l, for a single Si NW.

4.3.3 Results and discussion

As mentioned earlier, with the fabrication technology described here, large and thick Si contact regions are connected to the recessed Si-NWs, which allows the formation of ohmic contact form easily. Thus over the contact area, increasing contact size has a limiting effect on the overall contact resistance when $L >> \lambda$. In order to measure the contact resistance of the Al electrode to Si-NW device after annealing, we did extensive characterization using dedicated structures based on the TLM, by forming microstructures with the same implanted dose, same contact size and metal as used for Si-NW structures for estimation of contact resistance. Figure 4.5 shows the microscope images of Si microwire (Si-MW) and Si-NW structures for contact resistance measurements. The only difference for Si-NW and Si-MW structures as shown in Figs. 4.5b, c is the size of wires in the center region of the figures.

Figure 4.6a shows a linear *I-V* curve measurements from Si-MWs with multiple lengths (13 μm, 18 μm, 48 μm), width of 4 μm, and implanted dose of 10^{13} cm^{-2}. The doping concentration over contact region is ~10^{18} cm^{-3} as simulated in section 4.2.3. The slopes of the *I-V* curve are calculated to be equal R_T and are correlated

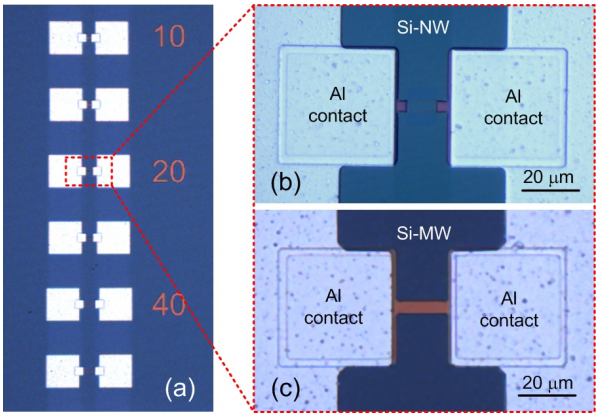

Figure 4.5 Microscope images of Si-MW vs. Si-NW structures based on TLM.

with the length of MWs in Fig. 4.6b. From Fig. 4.6b, we extract the contact resistance R_c of ~ 4.4 kΩ/contact, transfer length λ = 2.1 μm and specific contact resistance $\rho_c = \lambda^2 R_s \approx 3.7 \times 10^{-4}$ Ω cm^2, with $R_s = w \times 2.1 \times 10^9 = 8.4 \times 10^3$ Ω/sq., where 2.1×10^9 Ω/m is the slope for linear fitting in Fig. 4.6b. Measurements show quantitative agreement with reported values for sintered Al contacts on *p*-type silicon with $N_a \sim 10^{18}$ cm^{-3} [19]. This low ρ_c occurs because Al is a p-type dopant, and some of the Al diffuses into the Si during the sinter step, and a heavily doped *p*-region is thus established under the Al-Si contact region[3]. Even lower contact resistivity of ~10^{-6} Ω cm^2 can be easily achieved by increasing the contact doping

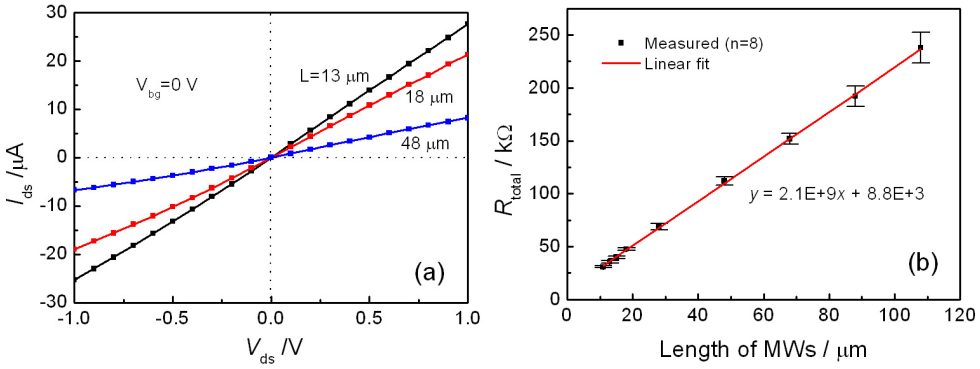

Figure 4.6 (a) Current-voltage measurements on Si-MWs (h = 190 nm, w = 4 μm) with V_{bg} = 0 V. (b) Total resistance plots as function of wire lengths.

concentration. However, for all Si-NW devices tested the contact resistance contributes to less than 1% of the total electrical resistance, with the resistance of Si-NW channel over MΩ scale and has been neglected in analytical conduction calculations (chapter 3).

4.4 Channel depletion of Si-NWs

4.4.1 The Si/SiO_2 interfaces

Since NWs have a very high surface-to-volume ratio, their electrical properties are extremely sensitive to the properties of the surface. Thus, when there is SiO_2 layer around NWs, the devices are strongly influenced by the Si/SiO_2 interface. The four types of charges associated with the thermally oxidized silicon structure are summarized in Fig. 4.7, including mobile impurity ions Q_m and radiation induced traps Q_{ot} present within the oxide layer, and fixed surface-state charge Q_f and fast surface state density D_{it} located at the Si/SiO_2 interface[3, 20]. Q_m is normally due to positive alkali ions in the oxide. These ions will drift under bias above 100 °C, or in some cases, at lower temperature, causing device instabilities.

All such impurities can be removed or complexed by a high temperature gettering step. However, precaution during device fabrication is considered a safer method for producing more stable and reliable devices. Radiation induced traps are caused by exposure to ionizing radiation. The radiation may occur during use of the device in radiation environments or during particular device processing steps, such as electron beam metallization, ion implantation, or sputtering of metals or dielectrics[20]. Q_{ot} can be eliminated by a low temperature (300 °C) anneal in an inert ambient. Q_f is positive stable charge in the SiO_2 layer near the interface caused by thermal oxidation. The value of Q_f/q can range from the low 10^{10} cm^{-2} to 10^{12} cm^{-2}, and depends on the annealing ambient and temperature represented by the Deal triangle[21]. Q_f reduces greatly when annealing at high temperature (e.g. 950 °C) in N_2 for 20 min, then levels off with increasing annealing time, and increases for long annealing times (> 60 min) at higher temperature 1200 °C[20]. Fast surface states derive their name from the fact that the traps responsible are in direct electrical communication with the silicon and thus respond rapidly to changes in surface potential. D_{it} increases with a high temperature annealing treatment and can be minimized by hydrogen annealing above 300 °C. All the charges and interface

states contribute to the silicon surface potential ψ_s, which influence the charge carrier density of Si-NWs[22]. Thus proper annealing steps need to be taken in order to optimize device performance.

The effect of fixed charges and interface states to Si-NW is less for higher doped device, thus larger for devices after OED, which results in a lower N_a. The Si/SiO_2 interface states are not included in the later discussion due to the large cross-sectional area of the present devices. For smaller lateral dimensions (~20 nm) with low doping levels (~10^{16}), typical interface state densities $D_{it}^{(100)}$~10^{10} cm^{-2} eV^{-1} and $D_{it}^{(111)}$~10^{11} cm^{-2} eV^{-1} [23], which can be either n- or p-type and acceptors or donors, can deplete the structure of all majority carriers and must be considered[22, 24].

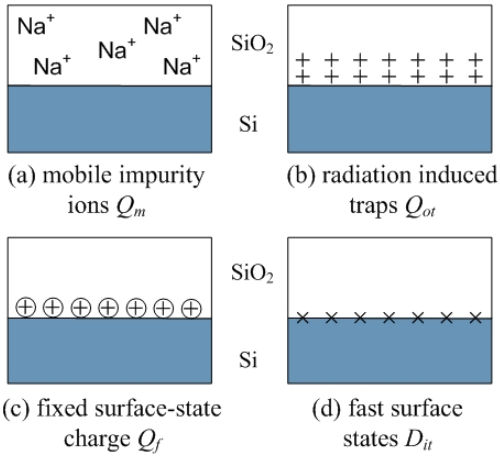

Figure 4.7 Charges and states associated with the Si/SiO_2 system.

4.4.2 Electrical measurements

The Si-NW devices presented have been fabricated in the ultra-clean line in the MESA+ cleanroom, which is designed for CMOS compatible fabrication processes, then subsequently annealed at 950 °C in N_2 for 20 min after the last oxidation step, and annealed in a H_2/N_2 5/95% forming gas at 450 °C for 20 min. The fabricated devices are depletion-mode variable resistance devices where the contact and channel regions are doped with the same impurity p-type. All the devices considered have dimensions greater than 50 nm, and therefore, their electronic behavior can be described classically. Electrical measurements were recorded in air on a probe station (PM8, Karl Süss) inside a Faraday cage using two

source measure units (2400, Keithley), one for the drain-source voltage (V_{ds}) and the second to sweep the back-gate contact voltage (V_{bg}). The source-measure units are controlled with the LabTracer2.0 software (Keithley).

4.4.3 Results and discussion

The Si-NWs presented here are depletion-mode field-effect devices and have been realized with different dimensions and impurity-doping concentrations using SOI wafers. Measured data in Fig. 4.8 show typical measured current-voltage (*I-V*) characteristics with and without back-gate biasing. Ideally for a Si-NW device, when the contacts are ohmic, and contact resistance are low, linear *I-V* curves should be obtained while both front-gate and back-gate are grounded, with the slope as total resistance of the NW and two contacts. However, that's not the case in our measurements. Figure 4.8a shows a depletion effect[25, 26], which requires V_{ds} > 1 V to open the Si-NW body channel allowing current to flow between the source and drain terminals with V_{bg} = 0 V. We attribute this channel depletion effect to fixed charge located in the front oxide near the top silicon device layer surface Q_{f_fo} and in the buried oxide near the bottom of the silicon device layer Q_{f_bo} due to the reactive thermal oxidation of the silicon surfaces (Fig. 4.8a). The fixed oxide charge is known to be positive and located near the Si/SiO_2 interface[21]. For p-type silicon, these fixed positive charges cause hole depletion in the silicon layer near the interface such that charge neutrality requires a negative charge in the silicon, which is provided by the ionized impurities of a depletion region $Q_f \sim N_a f_d$, where N_a is the impurity concentration and f_d is the depletion width. Applying a negative potential across the interface using V_{bg}, with respect to V_{ds}, reduces the extent of f_d, and therefore, the channel becomes partially depleted and results in linear *I-V* characteristics for all values of V_{ds} (Fig. 4.8b).

Figure 4.8c shows how the partially depleted region increases as V_{bg} increases negatively from plot-*i* to plot-*iv* (back-gate electrode is symmetrically located on the bottom of the buried oxide layer); results of two-dimensional finite element simulations (Taurus Medici, Synopsys). It should be noted that the maximum depletion width for a silicon layer doped with $N_a \sim 10^{16}$ cm^{-3}, is $f_d \sim 300$ nm which can easily deplete the NW device of majority carriers when all three interfaces are considered. As V_{bg} is increased negatively the non-depleted region becomes larger compared to the depleted region. The last contour plot shows the largest non-depleted

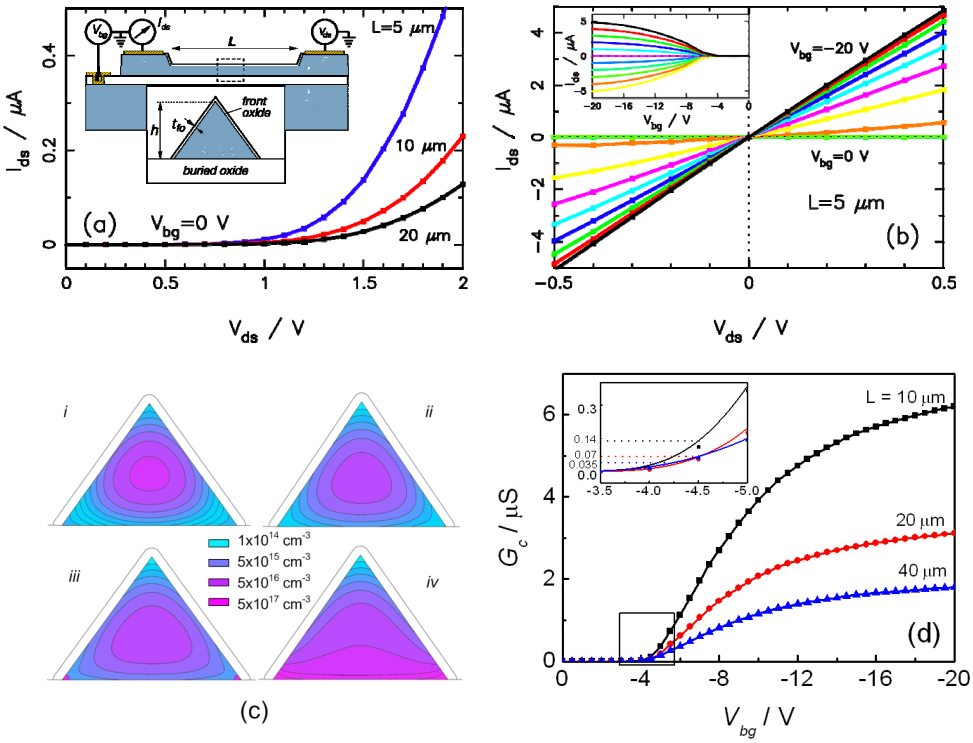

Figure 4.8 Measured Si-NW electrical characteristics (device height: h = 140 nm) (a) I_{ds} as a function of V_{ds} with V_{bg} = 0 V for devices with lengths L = 5 μm (blue), 10 μm (red) and 20 μm (black). (b) I_{ds} as a function of V_{ds} with -20 V ≤ V_{bg} ≤ 0 V in steps of 2 V. Inset: symmetric response as a function of V_{bg} for several V_{ds} values. (c) Calculated hole concentration in a Si-NW cross-section as V_{bg} is increased negatively (*i-iv*) using a two-dimensional finite element simulation with $Q_{f\_fo} = 2 \times 10^{11}$ cm^{-2}, $Q_{f\_bo} = 5 \times 10^{11}$ cm^{-2}, $N_a \sim 10^{17}$ cm^{-3} (uniform), t_{fo} = 10 nm and t_{bo} = 100 nm with the back-gate electrode located on the bottom edge of the buried oxide layer. (d) Measured channel conductance. Black squared region amplified in the insets: dashed lines represent ideal channel conductance for each length assuming $N_a \approx 1.5 \times 10^{16}$ cm^{-3}, $\mu_h = 400$ cm^2 V^{-1} s^{-1}.

region, which includes the formation of a hole accumulation layer in the silicon layer near the interface that explains large measured channel conductances for large negative V_{bg} (Fig. 4.8d).

The channel conductance of Si-NWs can be estimated as $G_c = (\mu_h |Q_c| - \mu_h |Q_d| + \mu_{eff} |Q_a|) L^{-1}$, where Q_c (C cm^{-1}) is the hole channel charge

per unit length, Q_d is the depletion charge, Q_a the accumulation charge (for a p-type material $Q_c > 0$, $Q_d < 0$ and $Q_a > 0$), and μ_{eff} is the field-effect hole mobility in the accumulation region. Based on measured device dimensions (with tapping mode atomic force microscopy imaging), the channel conductances of non-depleted Si-NWs with uniform doping concentration $N_a \approx 1.5 \times 10^{16}$ cm^{-3}, h = 140 nm, and L = 10 μm, 20 μm and 40 μm are $G_c \approx$ 140 nS, 70 nS and 35 nS, respectively, which are an upper limit for a non-depleted cross-section since the bulk hole mobility value is used and interface effects are not considered. Figure 4.8d shows the measured conductances as a function of V_{bg}. The measured conductance matches the estimated conductance of non-depleted Si-NWs of each length with $V_{bg} \approx$ -4.5 V, -4.5 V, and -4.2 V respectively (dashed lines in Fig. 4.8d inset). For V_{bg} = -20 V, the measured conductance increased to $G_c \approx$ 6.2 μS, 3.1 μS, and 1.8 μS, well beyond the estimated conductance. From calculations in Fig. 4.8c and measurements in Fig. 4.8d, it is clear that the addition of the accumulation charge contributes to the increased channel conductance beyond the estimated upper conductance limit for non-depleted structures. This discussion highlights the importance of the three-dimensional shape of nanostructures with respect to surface and interface effects due to the large surface to volume ratio.

4.5 Conclusion

This chapter described three important aspects of advanced fabrication techniques, including NW doping, contact formation, interface charge reduction and electrical measurements to characterize these properties. The doping profile of Si-NW device can be controlled by the implantation dose, energy and annealing step afterwards. There can be some improvement for the device fabricated, e.g. forming gate oxide by low temperature oxide deposition. The contact we obtained are ohmic, with resistance of ~ 4.4 kΩ/contact, which contributes to less than 1% of the total electrical resistance, and is neglected in analytical conduction calculations. The formation of Si/SiO_2 causes channel depletion, and has a huge effect to the *IV* characteristics. These three aspects also indicate the main differences from fabricating a NW structure to a NW electrical working device. Therefore, in order to optimize the electrical performance of NW devices, fabrication process needs to be carefully designed.

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Chapter 5

Electrochemical/Electrical Modeling and Sensitivity/Noise Analysis

The electrochemical/electrical behavior of the Si-NW sensor in solution is developed and discussed in this chapter. A simple two-dimensional (2D) analytical model has been developed and used to describe the conductance behavior of triangular multi-gate Si-NW devices, which is fit to experimental conductance measurements. A three-dimensional (3D) numerical model is developed and simulated with a finite-element solver, and is compared with the results obtained with the 2D analytical model. Two definitions of sensitivity are introduced, followed by discussions about the important device parameters, e.g. NW size (cross-sectional diameter), doping, gate oxide thicknesses, and noise, all of which influence the sensor sensitivity.[iv]

[iv] Partially modified from S. Chen, J.G. Bomer, E.T. Carlen, and A. van den Berg, *Nano Lett.* 11, 2334-2341, 2011 and M.N. Masood, S. Chen, E.T. Carlen, and A. van den Berg, *ACS Appl. Mater. Interfaces* 2, 3422-3428, 2010.

5.1 Introduction

With the rising popularity of Si-NW biomolecular sensors, the theoretical understanding of device behavior is becoming crucial for improving the detection sensitivity. Both experimental and simulation results have shown the advantages of using Si-NW sensors[1-3], which have higher detection sensitivity compared to their macroscale counterparts due to their high surface-to-volume ratio. To date, the lowest detection limit for deoxyribonucleic acid (DNA) hybridized to peptide nucleic acid (PNA) probes attached to the oxide surface is ~10 femtomolar using carefully designed devices and measurements[4, 5]. To further improve the detection sensitivity, Park et. al.[6] demonstrated that by decreasing the impurity doping concentration the sensitivity increased greater compared to reducing the device diameter. However, there are still questions worthy of discussion: Is smaller the better? How is the sensitivity influenced by parameters other than diameter, e.g. doping concentration, gate oxide thickness, and noise? Where is the scaling limit such that the technological difficulties outweigh detection sensitivity improvements? Although scaling the device diameters to nanoscale dimensions significantly reduces the sensing surface area and can severely limit the number of target molecules from a solution volume that reach the nanowire sensors, we will not consider this limitation and refer the reader to recent reports of active target concentration near the NW sensors[7, 8]. In this chapter, we explore the basic electrochemical and electrical behavior of Si-NW devices using 2D analytical and 3D numerical models, and discuss the posed questions.

5.2 Si-NW electrochemical/electrical modeling

Electrochemical silicon field-effect sensors are similar to conventional metal-oxide-semiconductor (MOS) devices where the front-gate metal is replaced with an electrolyte solution and reference electrode, thus forming the electrolyte-oxide-semiconductor (EOS) structure (Figure 5.1a); the reference electrode electrically biases the solution, which results in a modified flatband voltage that represents the mechanisms responsible for energy band bending at the silicon/front-oxide interface $V_{fb} = E_{ref} - \varphi_{Si}q^{-1} - \psi_o - Q_f/C_{ox} - Q_{it}/C_{ox} + \chi^{sol}$, where E_{ref} is the reference electrode potential, $\varphi_{\text{Si}}q^{-1}$ is the silicon work function, ψ_o is the potential at the

electrolyte-insulator interface, Q_f and Q_{it} are the fixed charge and interface state density near the silicon/front-oxide interface, and χ^{sol} is the dipole potential of the solution[1]. A partially depleted Si-NW device with the substrate and one device contact grounded (v_s = V_{bg} = 0V) can be approximated with the physical electrochemical representation as

M | Si-NW | front-oxide | electrolyte | reference electrode | M'

where ***M*** is the metal electrode and ***M'*** is the contact to the reference electrode. The silicon substrate of the Si-NW devices is biased with voltage source V_{bg} and the NW is biased with voltage source v_{ds}. For fully depleted Si-NWs, the full substrate structure, including the buried oxide and substrate layers, must be included in the electrochemical model.

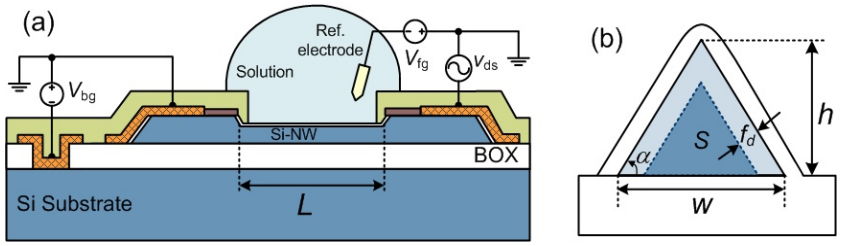

Figure 5.1 (a) Si-NW sensor configuration in solution with reference electrode with length *L*. (b) Width cross-section of a triangle Si-NW with height *h*, width *w*, triangle base angle α, and conduction area *S* (dark blue).

An inorganic dielectric material, such as silicon dioxide (SiO_2) and aluminum oxide (Al_2O_3), used as the gate-oxide and interface between the silicon and the solution is commonly used as a chemical sensing surface where the electrical properties of the sensor are sensitive to the ion concentration in the solution. For example, a SiO_2 front-oxide surface in contact with an aqueous electrolyte solution that is hydrated to form silanol surface groups, may be positively charged, negatively charged, or neutral depending on the bulk solution pH, surface composition, crystal orientation, and degree of hydration.

Assuming that only hydroxyl groups react with the electrolyte, the oxide surface in solution can be described by the site-binding model[9], which describes the relationship between the bulk pH, oxide surface charge density σ_o (C cm^{-2}) and

surface potential ψ_o (mV). Chemical sensing is achieved when a surface potential change $\Delta\psi_o$ is induced by a pH change in the bulk solution, or due to the addition of a specific ion, which results in a measurable conductance change ΔG via a field-effect across the dielectric layer. The fact that $\Delta\psi_o$ is dependent on the bulk pH of the electrolyte (through $\Delta\sigma_o$) forms the basis of the ion sensitive field-effect transistors (ISFETs)[10-12] pH sensors, which will be explained extensively in Chapter 6.

A biosensor on the other hand, typically consists of receptor molecules, commonly called ligands, attached directly to the surface of the sensing device; the ligands can be either a chemical or biological recognition element. Conventional Si-NW biosensors have the ligands attached directly to the SiO_2 sensor surface using silane-based attachment chemistry and more advanced approaches attach the ligands directly to the silicon surface through a covalent Si-C linkage[13]. The inherent detection sensitivity is due to the induced electronic charges on the oxide surface, an effective dipole due to the polar monolayer and/or dipole[14], and interface state density of the silicon/front-oxide interface. Biosensing is achieved when molecular binding at the sensing surface induces a surface potential change $\Delta\psi_o$ that results in a measurable conductance change ΔG via a field-effect across the dielectric layer. Detection sensitivity of ligand-analyte binding is dependent on the distance from the charged analyte to the silicon surface, which includes analyte, ligand, and linker (covalently attached to the front oxide surface in the conventional case).

In both cases, the surface charge density can be approximated in the first order with use of the Grahame equation $\sigma_o = (8\varepsilon_w\varepsilon_o kTn_o)^{1/2}\sinh(q(2kT)^{-1}\psi_o)$, for small values of ψ_o, which relates the surface charge density to the surface potential in a monovalent electrolyte, where ε_w is the dielectric constant of water, ε_o is the permittivity of free space, k is the Boltzmann constant, T is absolute temperature, and n_o is the buffer ionic concentration. Since the Si-NW field-effect sensors detect a surface charge density change $\Delta\sigma_o$, then it is important to consider how the target biomolecules are screened by dissolved ions in the buffer solution, which can significantly reduce $\Delta\sigma_o$ (i.e. $\Delta\psi_o$) that is induced by biomolecular binding. The Debye length is a measure of the distance that the dissolved ions extend away from the surface and for a symmetric monovalent electrolyte is defined as $\lambda_D = (\varepsilon_w\varepsilon_o kT$

$(2z^2q^2I)^{-1})^{1/2}$, where z is the valence ionic charge and I (M) is the ionic concentration. In general, to prevent charge screening we need $\lambda_D > l_R$, where l_R is the total length of the ligands[15-17]. Table 1 shows an example of the Debye lengths of a monovalent electrolyte.

Table 1 Calculated Debye lengths in a monovalent electrolyte.

I (M)	λ_D (nm)
10^{-6}	310
10^{-3}	9.7
1	0.3

The Si-NW sensors analyzed here are p-type depletion-mode devices, similar to the recently reported junctionless transistor[18], and therefore, are ideally *normally-on* for an applied v_{ds}. Gating the depletion-mode devices is similar to a junction field-effect transistor[19], with the exception that the depletion layer width is modulated with the field effect at the front-gate (FG) and/or the buried oxide (BOX) region with back-gate (BG). The conductance of the Si-NW device can be changed with the FG voltage source V_{fg} and/or with the surface potential ψ_o of the front oxide (FOX), which is a function of the surface charge density. As V_{fg} and/or ψ_o are varied positive and negative, the Si-NW conductance spans the depletion and accumulation modes, respectively. With a multi-gate structure, the BG controls the depletion behavior of the bottom side of the channel, and the FG controls the upper sides in contact with the solution using a calibrated reference electrode.

Figure 5.2 shows the NW width cross-sections and band diagrams representing each of the operating regions. In practice, a moderately doped p-type Si-NW is initially depleted due to the fixed charge Q_f and interface states Q_{it} near the FOX/Si interfaces, which typically results in a positive surface potential and space-charge region (SCR) (Fig. 5.2, $\psi_s > 0$), which effectively reduces the channel conductance G due to a decreased conductance cross-sectional area S. With additional positive charge at the FOX surface, the SCR further increases due to increased hole depletion, and therefore, G further decreases (Fig. 5.2, $\psi_s > \psi_o$). In the depletion region, G depends on the device dimensions: width w, length L and height h (Fig. 5.1), doping concentration N_a, and dopant concentration dependent bulk hole mobility μ_b[19].

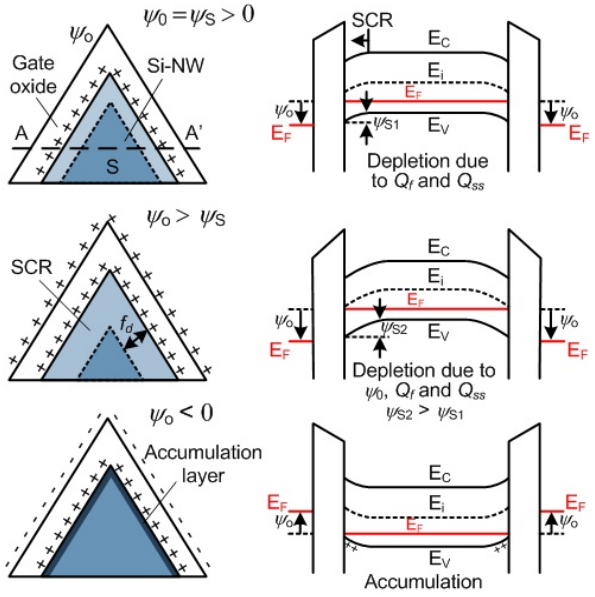

Figure 5.2 Operating regions of the depletion mode p-type triangular Si-NW and associated energy-band diagrams along the A-A' cross-section.

5.3 Two-dimensional analytical conductance model

The channel conductance of two parallel NWs with triangular cross-section operated in the depletion region can be approximated as $G = q\mu_b N_a L^{-1} S$, where S is the conduction cross-sectional area of the triangular Si-NW (Fig. 5.1c) with length L. From Fig. 5.1c, the conductance cross-sectional area of a single NW can then be written as a function of the depletion distance $S(f_d) = (\mathrm{w} - 2f_d/\sin\alpha)(h - f_d/\cos\alpha)/2$, where f_d is the depletion width distance function describing the two-dimensional depletion of the upper surface, which is a function of the oxide surface potential ψ_o. Therefore, the conductance of two parallel devices is

$$G = q\mu_b N_a L^{-1}(w - 2f_d/\sin\alpha)(h - f_d/\cos\alpha) \tag{5.1}$$

The depletion function can be approximated assuming a flat surface and the depletion approximation. The silicon surface potential ψ_s is related to V_{fg} by

$$V_{fg} = V_{fb} + \psi_s + Q_s/C_{ox} \tag{5.2}$$

The surface potential $\psi_s = qN_a f_d^2/(2\varepsilon_{Si}\varepsilon_o)$, where ε_{Si} and ε_{ox} are the relative permittivity of silicon and oxide, respectively, is a function of the depletion region width f_d and Q_s/C_{ox} is the potential drop over the FOX layer, where $C_{ox} = \varepsilon_{ox}\varepsilon_o/t_f$ is the FG capacitance per unit area and t_f is the FOX thickness (note: the reference electrode potential and ψ_o are lumped into V_{fb}). The charge per unit area in the semiconductor layer is $Q_s = qN_a f_d$ for a single surface. Substituting the expressions for ψ_s and Q_s/C_{ox} into Eq. 5.2 results in

$$V_{fg} = V_{fb} + qN_a f_d^2/2(\varepsilon_{Si}\varepsilon_o) + qN_a f_d t_f/(\varepsilon_{ox}\varepsilon_o) = 0 \tag{5.3}$$

and rearranging gives

$$f_d^2 + \frac{2\varepsilon_{Si}t_f}{\varepsilon_{ox}} f_d + \frac{2\varepsilon_{Si}\varepsilon_o}{qN_a}(V_{fb} - V_{fg}) = 0 \tag{5.4}$$

Solving Eq. 5.4 results in the depletion region width of a single surface

$$f_d = \left(\gamma^2 t_f^2 + 2\varepsilon_{Si}\varepsilon_o\left(V_{fg} - V_{fb}\right)/qN_a\right)^{1/2} - \gamma t_f \tag{5.5}$$

which is a function of $(V_{fg} - V_{fb})$, where $\gamma = \varepsilon_{Si}\varepsilon_{ox}^{-1}$ [13]. The triangular NW is fully depleted (S = 0 m^2) when the depletion region reaches a maximum value $f_{d,max} = h\cos\alpha$. For the triangle Si-NWs presented in this thesis with h = 140 nm, the maximum depletion width is $f_{d,max}$ = 81 nm, which corresponds to $\Delta\psi_o \approx 680$ mV with t_f = 5 nm and $N_a = 10^{17}$ cm^{-3}. For this analysis, we assume that the BOX/Si interface is not depleted and the BG is not electrostatically coupled to the front-gate, which is accomplished in practice by choosing an appropriate V_{bg}. As ψ_o is made increasingly negative, the channel becomes non-depleted (f_d = 0), which is the flat-band condition of the upper surface, defined as $V_{fg} = V_{fb}$, and an accumulation layer of majority carriers, holes in the case of a p-type layer, forms at the silicon surface with further decreasing ψ_o (Fig. 5.2, $\psi_o < 0$). The resulting channel conductance is then the sum of the conductance of the channel and the accumulated holes at the upper surfaces $G = q\mu_b N_a L^{-1} w + 2\eta\mu_a W_a L^{-1} Q_a$, where η is a scaling factor as the accumulation is not uniform near the tips of the triangular structure, μ_a is the field-dependent accumulation layer mobility[20], $W_a = (h^2 + w^2/4)^{1/2}$ is the width of a single upper surface, and $Q_a \approx \left(2\varepsilon_{Si}\varepsilon_o N_a kT\right)^{1/2}\left(e^{-\psi_s\lambda^{-1}} + \psi_s\lambda^{-1} - 1\right)^{1/2}$ is the accumulation charge per unit area for a

p-type material. Therefore, the depletion mode channel conductance can be generalized in both operating regions

$$G = q\mu_b N_a L^{-1}\left(w - 2f_d/\sin\alpha\right)\left(h - f_d/\cos\alpha\right) + 4\eta\mu_a W_a L^{-1} Q_a \begin{cases} Q_a = 0, & V_{fg} > V_{fb} \\ f_d = 0, & V_{fg} < V_{fb} \end{cases} \quad (5.6)$$

It should be noted that the metal/semiconductor contact region has been carefully designed and characterized to have a negligible contribution to the total device conductance (< 1%), and therefore, has been neglected in the conductance model derivation[21]. The model was fit to the measured I_{ds} as a function of V_{fg} (against a Ag/AgCl reference electrode) for various v_{ds}. The model parameters used to fit the I_{ds}-V_{fg} data are $N_a = 6 \times 10^{16}$ cm^{-3}, $V_{fb} \approx$ -1.1V, $\mu_b \approx 186$ cm^2 V^{-1}s^{-1}, $\eta \approx 0.7$. Figure 5.3a shows the excellent match between the model (solid lines) and measured data (markers) over both the depletion and accumulation regions.

The analytical model developed here is valid for heights down to h~50 nm. Approximately 600 mV is required to completely deplete the NWs from the flat-band condition at low v_{ds}, which is a reasonable value considering a maximum depletion width of $f_{dm} \approx 77$ nm for $t_f = 20$ nm with $N_a = 6 \times 10^{16}$ cm^{-3}. Figure 5.3b shows an example of the transconductance $g_m = \partial I_{ds}/\partial V_{fg}\big|_{V_{ds}}$ of the measured I_{ds}-V_{fg} data. The transconductance increases for increasing negative V_{fg} and reaches a maximum for V_{fg} slightly more negative than the estimated flat-band $V_{fb} \approx$ -1.1 V

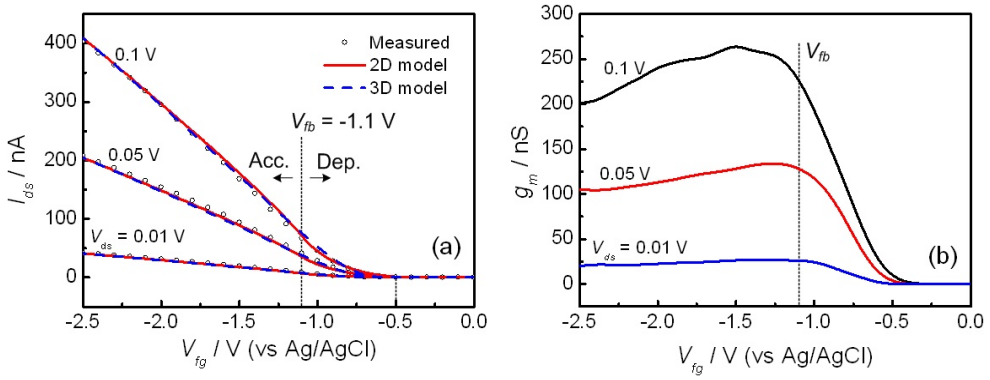

Figure 5.3 (a) Measured (open markers), analytical 2D model (solid red line) and numerical 3D model of Si-NW I_{ds} as a function of applied V_{fg} for different v_{ds} (V_{bg} = 0V); (b) Transconductance and location of V_{fb} calculated from measured I_{ds}-V_{fg} data.

for different v_{ds}, and subsequently decreases for larger negative V_{fg} due to the field dependent hole mobility for increased V_{fg} and accumulation layer screening. The transconductance is largest for slightly accumulated surfaces, which is used as the operating point of the sensor in many cases[21, 22].

5.4 Three-dimensional numerical conductance model

A three-dimensional (3D) Si-NW numerical model has been simulated with a commercial finite element TCAD solver (Sentaurus, version D-2010.03, Synopsys) as a comparison to the 2D analytical model. The 3D NW structures have been created with a commercial process simulation code (Sprocess, Synopsis) using the deposition and etching functions, which finally results in parallel NWs with triangle cross-sections that resembles the fabricated Si-NW device as shown in Fig. 5.4a. The silicon device layer is uniformly doped with boron with $N_a = 6 \times 10^{16}$ cm^{-3}, t_b = 200 nm and t_f = 20 nm. At both ends of the NW, there are two large contacting areas that form the metal contacts. An ideal gate above the front oxide is used for controlling the NW surface potential (Fig. 5.4b). The electrical behavior of Si-NW devices have been numerically simulated with commercial code (Sdevice, Synopsis), in which the electrostatic potential is solved by the Poisson equation, and the carrier transport is modeled by the drift-diffusion model[23].

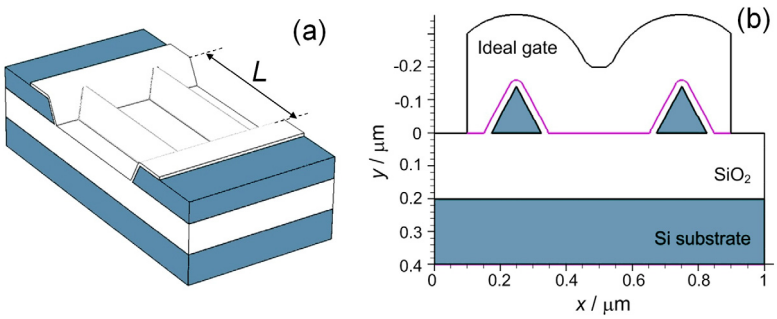

Figure 5.4 (a) 3D structure of a Si-NW device with parallel triangle NWs with length L. (b) Width cross-section of Si-NWs, where the purple line indicates the front gate contact interface.

Figures 5.3a show experimental and simulated (2D analytical and 3D numerical) I_{ds}-V_{fg} curves. The geometry parameter used for the 3D numerical model is the

same as those used for the 2D analytical model, with h = 140 nm and L = 7 μm, the same doping concentration and front gate oxide thickness. The electrical behavior is modeled without fixed interface charges or surface states. In both models the mobility has been adjusted to fit the measured data. The front-gate voltage V_{fg} has been shifted to match the flat-band voltage V_{fb} of the measured data. Figure 5.3a shows the excellent fitting of simulated result to the measured I_{ds} as a function of V_{fg} (vs. Ag/AgCl reference electrode) for various v_{ds}. These results show the accuracy of 2D analytical model while demonstrating the feasibility of using 3D numerical model for the Si-NW sensitivity estimation/comparison in section 5.5.

5.5 Sensitivity and noise analysis

In this section we analyze the sensitivity of Si-NW biosensors from the perspective of the entire sensing system, which includes the Si-NW sensors, probe molecules attached to the sensing surface, buffer solution, reference electrode, and conductance measurement method. In other words we consider the entire measurement system. In addition, we discuss the previously posed questions with results from either analytical calculations or numerical simulation with respect to how the detection sensitivity is influenced by NW size, doping concentration, gate oxide thickness, shape, and interface condition by numerical simulation.

The formal definition of sensitivity is the ratio of change in the response (or measured output) of the measurement system to a change in the stimulus (or system input)[24]. This definition can be interpreted as the slope of a calibration plot of output response versus input stimulus. An alternative definition of sensitivity is related to the limit of detection[25]. We will use the former definition which is related to the ratio of the measured output response change ΔR to the applied input variable change ΔV: $S_{RV} = \partial R/\partial \mathrm{V} \approx \Delta R/\Delta V$. The terms of the sensitivity expression can be mathematically transformed, for example variables R and/or V can be transformed to a log scale. The quantitative resolution of the measurement can be estimated as $Q_R = \varepsilon_R/S_{RV}$, where ε_R is the uncertainty of the measured response ΔR[26]. We consider two types of Si-NW sensors: pH chemical and surface hybridization biochemical sensors. The Si-NW pH chemical sensors measure the potential difference ψ_o across the electrical double layer at the interface between an electrolyte solution and an oxide surface, which is related to the activity (or concentration) of the potential determining (p.d.) ions. For an oxide surface, the H^+

ion is p.d., which is assigned to the oxide surface, and counter ions present in solution are from the background electrolyte and can be neglected at low ionic concentrations. The bulk pH is related to the H^+ ion activity and the experimental measurement of ψ_o is obtained through titration of the oxide in the presence of a supporting electrolyte by changes in the bulk pH, and therefore, the sensor input stimulus is $\Delta V = \Delta\text{pH}$ and the measured output is $\Delta R = \Delta\psi_o$, which results in a sensitivity of $S_{\text{pH}} = \Delta\psi_o/\Delta\text{pH}$ (mV/pH). It should be noted that the measured output is actually device conductance and the surface potential is extracted from the $\Delta\psi_o$-ΔG calibration curve, such that the sensitivity can be compared to other types of the sensors. The pH chemical sensors are described in more detail in Chapter 6.

The Si-NW biomolecular sensors measure surface potential changes due to the hybridization of charged target biomolecules, such as DNA, to surface receptor molecules, such as complementary DNA or PNA, attached directly to the sensing surface. At the highest level of abstraction, the sensitivity of this biosensor system is $S_{\text{DNA}} = \Delta G/\Delta[C]_{\text{DNA}}$, (nS/M), where $[C]_{\text{DNA}}$ is the concentration of the target DNA, which is essentially the slope of the measured conductance G versus target analyte concentration $[C]_{\text{DNA}}$. Since the target biomolecules hybridize to the probe molecules on the sensing surface result in a change in the net surface charge density $\Delta\sigma_o$, then the surface potential can be estimated $\psi_o = \gamma^{-1}\sinh^{-1}(\sigma_o (8\varepsilon_w\varepsilon_o kT n_o)^{-1/2})$. The estimation of the surface charge density requires consideration of how the charged molecules are arranged on the surface, length of any linker molecules, pH of the bulk solution as the oxide has some intrinsic charging in an electrolyte (typically assume to be $\sim 8\times10^{-5}$ C cm^{-2}), and intrinsic electronic charge of the receptor molecule. For example, Fritz *et al.* estimated that a surface potential change $\Delta\psi_o = 3$ mV resulted from the hybridization of 3×10^4 12-mer oligonucleotide molecules per μm^2 (corresponding to a target concentration of ~20 nM) from complementary DNA probe molecules lying on a flat surface covered with a positively charged poly L-lysine layer[27]. For this type of estimation, the orientation of the hybridized complex is important[28]. Therefore, it is reasonable to use an alternative sensitivity metric $S_{\psi o} = \Delta G/\Delta\psi_o$, which can be estimated directly by recording a calibration plot of conductance versus front-gate volgate.

There have been two definitions of sensor sensitivity in Si-NW literature: transconductance g_m and normalized conductance change $\Delta G/G_o$, where $\Delta G =$

$G(\Delta\psi)$-G_o and G_o is the quiescent bias conductance. The transconductance was previously defined as the differential change of output (current through NWs) with differential change of front-gate voltage, where V_{fg} is the voltage applied to the reference electrode of the measurement, and the maximum g_m can be considered as the largest gain provided by the sensor. The transconductance corresponds to $S_{\psi o}$ through the relationship between V_{fg} and V_{fb} (Eq. 5.2). The normalized conductance is an important metric, however, from a measurement perspective. For single NW measurements the devices are typically biased with a quiescent conductance G_o. If G_o is too large then there is a lower limit that the measurement equipment can measure ΔG. Therefore, it is advantageous to find a biasing regime that maximizes $\Delta G/G_o$ such that the small values of ΔG can be resolved with the measurement system. Over the subthreshold region, the drain current varies exponentially with gate voltage, and the sensitivity turns to be the highest in terms of the relative change in the normalized conductance change $\Delta G/G_o$[29]. The slope of the exponential falloff gives a device parameter defined as the gate swing $S_{sub} = \mathrm{d}V_{fg} / \mathrm{d}(\log I_{ds})$, which is the gate potential needed to reduce the current by one decade. Two terms, threshold voltage and subthreshold current, need to be defined as to avoid confusion with previously definitions of subthreshold device operation. The threshold voltage V_T is the voltage applied to the gate of a field-effect transistor that produces a measurable current from drain to source. For a normally-off device, V_T is also referred to the turn-on voltage. The conductance region below V_T, which is typically extrapolated to gate voltage bias axis once a near-linear log G vs V_{fg} behavior is achieved, is the subthreshold region, where the drain current is very small and varies exponentially with gate-to-source voltage[30]. In the following sections, various parameters are listed and how these parameters influence g_m and $\Delta G/G_o$ are discussed.

For Si-NWs with large size or high doping, complete depletion of devices becomes difficult, in which case, the $\Delta G/G_o$ is small due to the large G_o. When the silicon surface potential ψ_s equals ~$2\psi_B$, strong inversion begins and the depletion width reaches a maximum, where ψ_B is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. Then we have

$$\psi_s \approx 2\psi_B = 2kTq^{-1}\ln(N_a n_i^{-1}) \tag{5.7}$$

where n_i is the intrinsic carrier density. The maximum depletion width for a flat surface is

$$f_{d,max} = \left(2\varepsilon_{Si}\varepsilon_o\psi_s (qN_a)^{-1}\right)^{1/2} \approx \left(4\varepsilon_{Si}\varepsilon_o\psi_B (qN_a)^{-1}\right)^{1/2} \tag{5.8}$$

Figure 5.6 shows how the $2\psi_B$ and $f_{d,max}$ vary with doping concentrations. Complete depletion will not happen when the height of a triangular cross-sectioned Si-NW is over a critical height $h_c = f_{d,max}/\cos\alpha$ ($2f_{d,max}$ for a square cross-sectional area) with a certain N_a due to the multigate NW structure, e.g. critical heights are h_c = 193 nm for $N_a = 10^{17}$ cm^{-3} ($f_{d,max}$ = 104 nm), and h_c = 65 nm for $N_a = 10^{18}$ cm^{-3} ($f_{d,max}$ = 35 nm). The effect of size and doping to the gate swing will be discussed later through 3D numerical simulation.

The Si-NW devices used for the sensitivity analysis consist of a single Si-NW per device with triangular cross-section as illustrated in Fig. 5.4b, with L = 1.0 μm, and are uniformly doped with boron ($N_a = 10^{17}$ cm^{-3}). The thickness of the buried oxide is 200 nm, and front gate oxide is t_f = 5 nm thick. There are a few items we assume in order to simplify the comparison of sensitivity for multiple sizes and doping profiles: 1) there is no fixed charge and interface state presents at the silicon/oxide interface, Q_f = 0 cm^{-2}, Q_{it} = 0 eV^{-1} cm^{-2}; 2) ideal front-gate material, no barrier between the Fermi level in the gate electrode and the intrinsic Fermi level in silicon. For all the front-gate scanning, V_{ds} = 0.1 V, V_{gs} = 0 V.

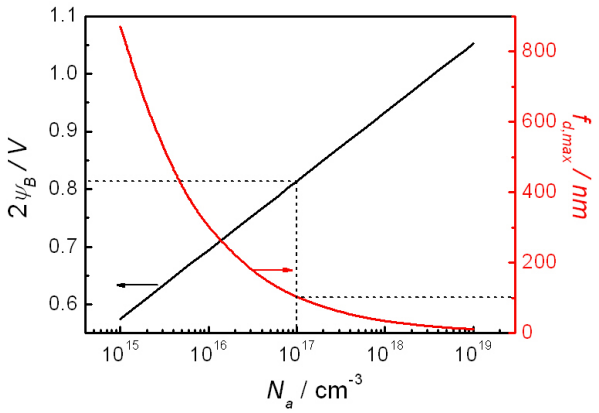

Figure 5.6 Variation of $2\psi_B$ and $f_{d,max}$ as a function of doping concentration at room temperature.

5.5.1 Size

Improved sensitivity has been shown by different research groups experimentally with the argument of high surface-to-volume ratio[31, 32]. The surface-to-volume ratio for a square NW is $3/h$, which increases dramatically with decreasing height. Figure 5.7a shows the comparison of gating behavior for different sizes of Si-NWs, from 20 nm to 500 nm, with the same doping 10^{17} cm^{-3}. The flat-band voltage is shifted towards negative value due to the work function difference between the doped silicon and gating material. In our case, it equals $\sim\psi_B$, which is a function of doping concentration, as there is no barrier between the gate electrode and the intrinsic silicon, with $V_{fb} = \psi_B = 0.41$ V for $N_a = 10^{17}$ cm^{-3}.

For small surface potential changes, such as DNA hybridization on an oxide surface ~3 mV[27], in the high transconductance region (V_{fg} = -0.56 V) for 100 nm Si-NW with doping of 10^{17} cm^{-3}, the current increased from 403 nA to 407 nA, with $\Delta I_{ds} \approx 4$ nA (1.1% of change), compared with $\Delta I_{ds} \approx 7$ nA (0.7% of change) for 200 nm and $\Delta I_{ds} \approx 0.9$ nA (1.4% of change) for 20 nm Si-NWs with the same doping as calculated from Fig. 5.7a. On one hand, g_m increases with device dimension due to the large bias current. On the other hand, the gate swing reduces with decreasing size, however, no improvement in the gate swing is observed with further reduction in size. The subthreshold region shows the same slope for size from 20 nm to 200 nm and reduced slopes for sizes over 200 nm due to the large base current for big NWs, which agree with the results obtained from Eq. 5.8. Figure 5.7b shows the ΔI_{ds} (left y axis) and $\Delta G/G_o$ (right y axis) as a function of V_{fg} for multiple surface potential changes. The $\Delta G/G_o$ value for $\Delta\psi_o = 3$ mV is the highest over the subthreshold region, and decreases dramatically over the depletion region, and then flattens out over the accumulation region. In order to have a high $\Delta G/G_o$ and a measurable current change $\Delta I_{ds} > 70$ pA, which is the typical root mean square amplitude of the current I_{ds} noise from the lock-in amplifier with a 300 ms integration time and will be discussed later in this chapter (Fig. 5.12a), a working region of -0.1 V $\leq V_{fg} \leq$ -0.5 V (for this case) is recommended that includes the depletion region and part of subthreshold region, as shown in Fig. 5.7b with V_{fg} in the shadowed region. Choosing a working region depends on a compromise between high $\Delta G/G_o$ and high ΔI_{ds} (or g_m) over this region.

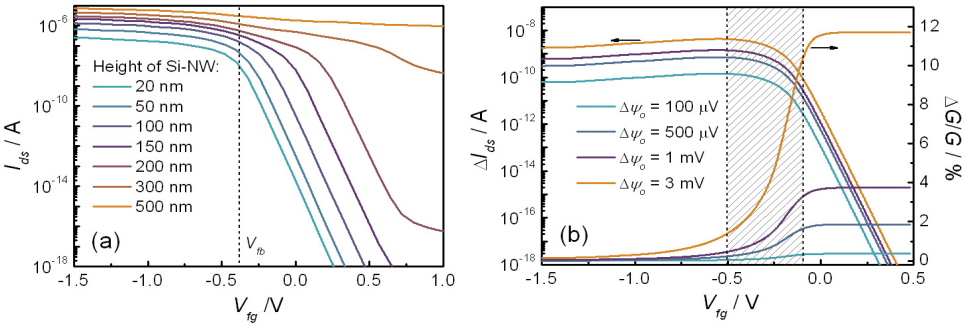

Figure 5.7 (a) Current change with front gate scanning for Si-NWs with the same doping 10^{17} cm^{-3}, and a range of sizes for 20 nm ≤ h ≤ 500 nm; (b) $\Delta G/G_o$ as a function of V_{fg} for Si-NW with h = 100 nm, with different $\Delta\psi_o$ (100 μV, 500 μV, 1 mV and 3 mV).

5.5.2 Impurity doping concentration

Figure 5.8 shows the comparison of Si-NW transconductance for the same height h = 100 nm, and with various boron doping concentrations N_a = 10^{16} cm^{-3}, 5 × 10^{16} cm^{-3}, 10^{17} cm^{-3}, 5 × 10^{17} cm^{-3}, 10^{18} cm^{-3}, and 5 × 10^{18} cm^{-3}, respectively. The peak g_m value, which occurs near the weak accumulation region, increases with decreasing doping concentration, and reaches a maximum value at N_a = 10^{17} cm^{-3}, then drops with further decreasing of N_a. This phenomenon is a compromise between the accumulation charge density Q_a and mobility μ_a, where Q_a scales with N_a, and μ_a scales inversely with N_a. The decreasing rate of g_m for certain doping outside the peak region reduces with increasing N_a. So in order to get the highest transconductance during operation, devices need to be well-designed, while both doping concentration and working region need to be taken into account. In case of wide working region needed, higher doping concentration is preferred. The distribution of g_m remains the same except shifts towards negative front gate voltage when the positive fixed charges present at the Si/SiO_2 interface. The same holds for the subthreshold region with S_{sub} not affected[33].

The gate swing S_{sub} for a Si-NW with h = 100 nm is similar for doping concentrations between 10^{16} cm^{-3} and 10^{17} cm^{-3} with S_{sub} = 62 mV/decade, and then increases with increasing doping concentration, as shown in Fig. 5.9a. Highly doped Si-NWs can achieve the same S_{sub} by decreasing the size. As shown in Fig. 5.9b, for 50 nm NW, reduced S_{sub} is observed for N_a = 5 × 10^{17} cm^{-3} and 10^{18} cm^{-3}

with a similar value as for the lower doping N_a = 10^{16} cm^{-3}, ~61 mV/decade. Size and doping influence S_{sub} differently and are crucial aspects for sensitive detection. For larger sizes (h = 100 nm), lower doping 10^{17} cm^{-3} is suggested to optimize the sensitivity; and for smaller sizes (h = 50 nm), the same S_{sub} can be achieved with higher doping (N_a = 10^{18} cm^{-3}).

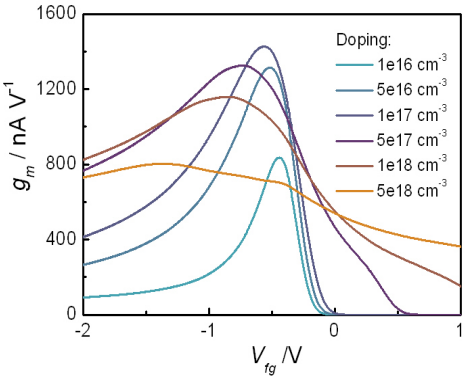

Figure 5.8 Transconductance comparison among Si-NWs with h = 100 nm and different doping concentration.

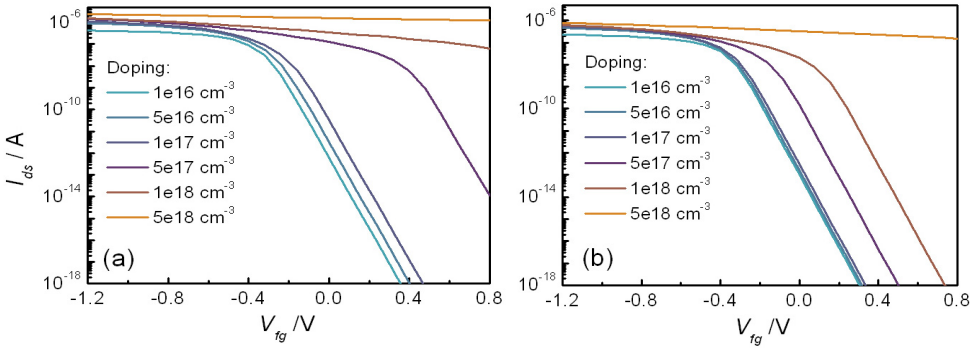

Figure 5.9 Current change with front gate scanning for nanowires with different doping and size of (a) h = 100 nm, (b) h = 50 nm.

5.5.3 Gate oxide thickness

Figure 5.10 shows the strong dependence of the depletion width to t_f and N_a that are calculated from Eq. 5.5 for fixed $\Delta\psi_o = V_{fg} - V_{fb}$ = 3 mV. The exponential decay of f_d with t_f illustrates that for N_a = 10^{17} cm^{-3}, the depletion width reduce dramatically

with $t_f > 10$ nm, compared with $t_f > 5$ nm for $N_a = 10^{18}$ cm^{-3}. For a depletion-mode Si-NW device, increased gate oxide thickness results in loss of sensitivity. Figure 5.11 shows the I_{ds}/g_m values with $t_f = 2$ nm, 5 nm, 10 nm, 20 nm and $N_a = 10^{17}$ cm^{-3} as a function of V_{fg}. The peak g_m values decrease with increasing gate oxide thickness, and drop from 1360 nA/V for 2 nm gate oxide to 284 nA/V for 20 nm gate oxide (Fig. 5.11 a). However, gate swings for all different gate oxide thickness remain similar (Fig. 5.11 b). Thus thin gate oxide (a few nanometers) is preferred for sensitive detection.

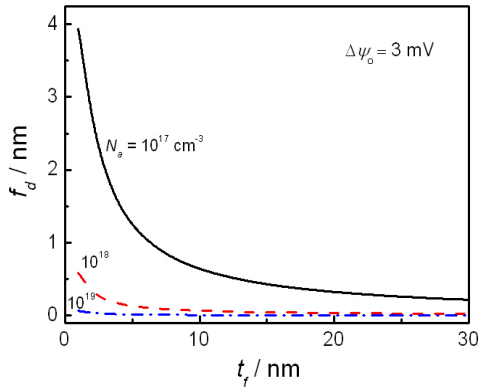

Figure 5.10 Depletion width change as a function of FOX thickness.

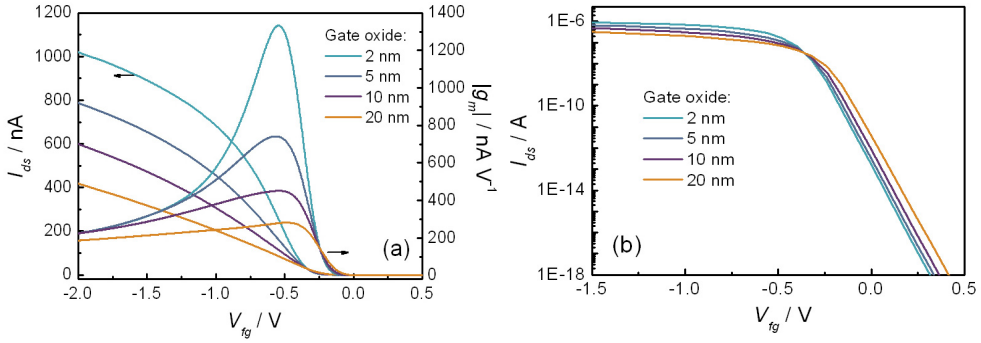

Figure 5.11 Front gate scanning for Si-NWs with 50 nm height, and gate oxide thickness range 2 nm ≤ t_f ≤ 20 nm: (a) current and transconductance vs V_{fg}, (b) current in logarithmic scale.

5.5.4 Noise

The Si-NW measurement system consists of many components that includes: the Si-NW sensor, electrolyte solution, reference electrode, voltage sources for applying the front-gate (V_{fg}) and back-gate (V_{bg}) bias voltages, and lock-in amplifier, with built-in modulation voltage supply (v_{ds}) to measure the conductance changes. Since the system noise is composed of the all the noise sources in the system, the lock-in amplifier is used to measure over a very small bandwidth at the modulation frequency using a quadrature operation, which ensures that the measured noise of the system is as small as possible. Figure 5.12 shows a typical example of the measured current from the Si-NW measurement system that is biased with a mean current of I_{ds} = 6.5 nA. The root mean square (rms) amplitude of the current noise is σ_{Ids} = 70 pA, which is related to the output uncertainty of the system and can be used to estimate the quantitative resolution of the system Q_R. The inset of Fig. 5.12 shows a histogram of the current noise from the measurement system. For a complete system sensitivity estimation then the system response can be measured with varying target molecule concentration, as described earlier.

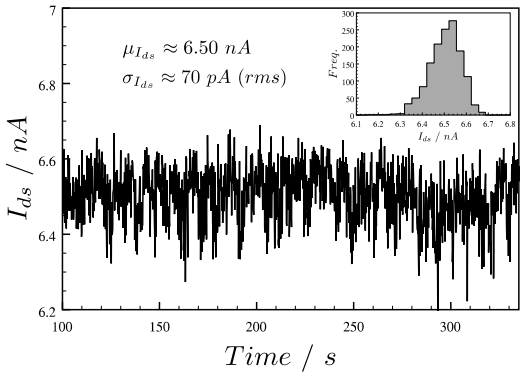

Figure 5.12 Typical noise measurement from Si-NW measurement system with 30 ms integration time from the lock-in amplifier

To get a measurable current change ΔI_{ds} > 70 pA, the minimum surface potential change is $\Delta\psi_o$ ~100 μV according to Fig. 5.7b, which correspond to ~1000 12-mer oligonucleotide molecules per μm^2. For triangular Si-NW with h = 100 nm, surface

area = 2.5 μm^2, which means we need at least 2500 molecules per Si-NW in order to have a detectable current change. For a sample volume of 1 μL, and assume all the molecules can be immobilized onto the Si-NW surface, this corresponding to a target concentration of ~4 fM.

An alternative approach is to use a differential measurement approach where a reference sensor is used to cancel common-mode noise sources. The differential measurement signal is then $G_{diff} = G_{sen} - G_{ref}$, where $G_{sen} = G_{ref} + \Delta G_{sen}$, and ideally $G_{diff} = \Delta G_{sen}$ where the conductance changes due to small surface potential changes can be resolved with higher precision than the single device measurements.

5.6 Conclusion

The electrical/electrochemical model is presented for describing the Si-NW EOS system. The simple 2D analytical expressions obtained show an excellent fitting to the experimental data, as well as the 3D finite-element model. With simulation, the influence of sizes, doping concentrations, fixed charges, gate oxide thicknesses, and noise level to the sensitivity are discussed. The way these parameters influence the sensitivity depends on which sensitivity definition is chosen, g_m or $\Delta G/G_o$. To get a high g_m, a relatively low doping concentration is preferred, e.g. 10^{17} cm^{-3}. However, it's difficult to use g_m for sensitivity comparison as it scales with size. To achieve a high $\Delta G/G_o$, a relatively large size and low doping concentration is preferred, e.g. height of 100 nm with doping of 10^{17} cm^{-3}.

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Chapter 6

NanoISFET with Near Ideal Nernstian Response

Silicon nanoISFET pH sensors are presented in this chapter. A comparison between the nanoISFET and the conventional ISFET is presented, which describes the similarities and differences in device structures and working principles. Extensive electrochemical testing of fabricated nanoISFETs has been conducted together with the development of electrochemical/electrical models describing the device behavior and performance. Three variations of a SiO_2 gate-oxide and an ALD Al_2O_3 gate-oxide have been deposited on the nanoISFETs and titration experiments were used to assess the pH behavior and sensitivity. A comprehensive analytical model of the nanoISFET sensor that utilizes the well-established Site-Binding Model (SBM) accompanies the experimental results. An extracted $\Delta pK \approx 1.5$ from the measured responses further supports the near ideal Nernstian pH sensitivity of 57.8 ± 1.2 mV/pH at 22 °C for ALD Al_2O_3 gate-oxide.[v]

[v]Modified from S. Chen, J.G. Bomer, E.T. Carlen, and A. van den Berg, *Nano Lett.* 11, 2334-2341, 2011.

6.1 Introduction

The number of reports of silicon nanowire field effect transistor (Si-NW FET) sensors has greatly increased over the last decade, which span a wide range of practical applications, for example, pH sensing[1-3], gas sensing[4, 5], flow velocity sensing[6], label-free biosensing[7-10], optoelectronics[11], and thermoelectrics[12]. Similar to the ion-sensitive FETs (ISFETs), which were first reported over forty years ago[13], Si-NW FET, or nanoISFET, sensors estimate surface potential changes of a solution/gate-oxide interface by measuring the conductance change of a multi-gate silicon layer in direct contact with the gate-oxide layer. The conductance change in the silicon layer is induced by an electric field generated across the gate-oxide by the surface potential change on the gate-oxide surface. Sensors that measure surface potential changes have many different applications including the hybridization of the charged biomolecules to surface attached probes[7, 8], gas sensing[4, 5], and pH sensing[3].

We present new nanoISFET pH sensors that are manufactured using top-down fabrication technology presented in chapter 3, which can be scaled down to sub-20 nm dimensions proportionally in all dimensions using conventional microfabrication methods[14], in contrast to previously reported top-down fabricated nanowires[15] that cannot be scaled down proportionally in all dimensions, and therefore, do not have a multi-gate structure for small dimensions. The new fabrication technology additionally provides the ability to control the nanowire impurity doping with high precision, and therefore, the depletion region that controls the conductance modulation in the depletion-mode devices is immediately adjacent to the gate-oxide sensing surface. Finally, all measurements are conducted using a conventional reference electrode in the supporting electrolyte, which provides an electrically stable sensing interface.

Three variations of a SiO_2 gate-oxide and an ALD Al_2O_3 gate-oxide have been deposited on the nanoISFETs and titration experiments were used to assess the pH behavior and sensitivity. Extensive electrical and electrochemical testing of fabricated nanoISFETs has been conducted together with the development of electrical and electrochemical models describing the device behavior and performance. The new nanoISFET pH sensors have near ideal Nernstian pH sensitivity on one of the highest reported for a field-effect type of sensor[16].

6.2 NanoISFET vs conventional ISFET

NanoISFET pH sensors measure the potential difference ψ_o across the electrical double layer at the interface between an electrolyte solution and an oxide surface, which is related to the activity (or concentration) of the potential determining (p.d.) ions that can be described with the Nernst equation $\psi_o = 2.303\lambda \log\left[a_{H^+}/a^o_{H^+}\right]$, where $\lambda = kTq^{-1}$, q is the elementary charge, k Boltzmann's constant, T is the absolute temperature, a_{H^+} is the ion activity of the solution, and $a^o_{H^+}$ is ion activity at the point of zero charge (pzc). Therefore, the maximum variation ψ_o can take is 58 mV per decade of ion activity at the standard temperature of 293 K (20 °C). For an oxide surface, the H^+ ion is p.d., which is assigned to the oxide surface, and counter-ions present in solution are from the background electrolyte and can be neglected at low ionic concentrations. The bulk solution pH, or pH_B, is related to the H^+ ion activity, and therefore, the experimental measurement of $\Delta\psi_o$ is obtained through titration of the oxide in the presence of a supporting electrolyte by changes in pH_B. The corresponding maximum pH sensitivity of a surface is, therefore, limited to $\Delta\psi_o / \Delta pH_B = 2.303\lambda$, which is a function of temperature such that the isotherms have a common pH value that coincide with the pzc of the electrode referred to as pH_{pzc}.

In principle, the nanoISFET sensors perform the same measurement as a conventional ISFET since both device configurations measure surface potential changes $\Delta\psi_o$ as a function of ΔpH_B, however the nanoISFETs have a multi-gate structure that can result in higher detection sensitivities. Figures 6.1a, b show the length cross-section diagrams of a p-channel enhancement-mode ISFET and a depletion-mode Si-NW respectively. The depletion-mode Si-NW is one of the most commonly used sensor configurations[7, 8]. The ISFET structure resembles a MOSFET except the metal gate is removed from the device and replaced with a reference electrode inserted in an aqueous solution which is in contact with the gate oxide[13]. The nanoISFET is different from the conventional ISFET in that the Si-NW channel is electrically isolated from the silicon substrate by a buried oxide (BOX) layer and the Si-NW is isolated from the electrolyte by the front oxide (FOX) layer. Both front-gate (FG) and back-gate (BG) voltages, V_{fg} and V_{bg}, respectively, are used to bias the quiescent conductance of the Si-NW.

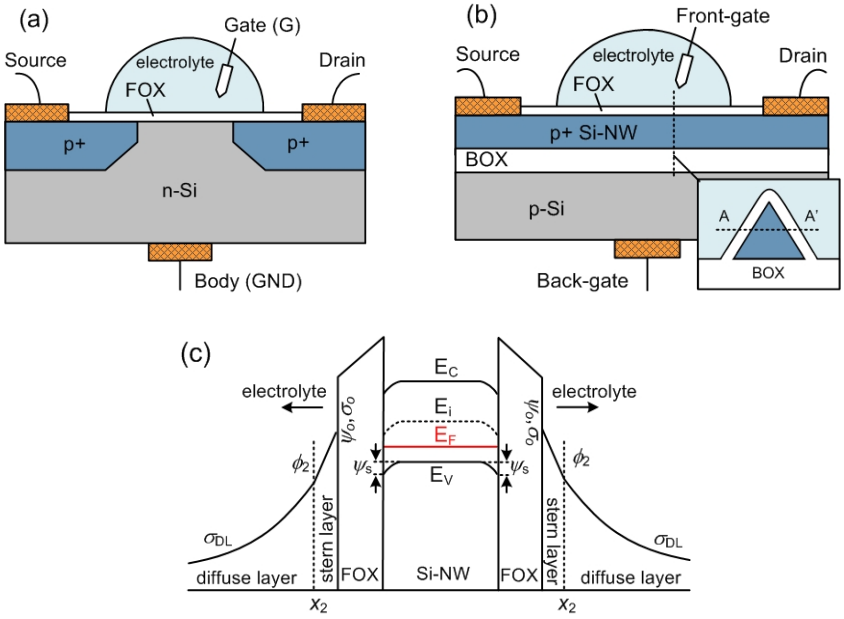

Figure 6.1 (a) Cross-section diagram of p-n-p ISFET. (b) Length cross-section diagram of homo-geneously p-doped Si-NW FET. Inset: triangular nanowire width cross-section (A-A'), FOX: front-oxide, BOX: buried oxide; (c) Potential profiles across electrolyte to the FOX surface and the energy-band diagrams of the p-type Si-NW width cross-section showing the silicon surface potential ψ_s.

The multi-gate structure of the Si-NW, shown in the inset of Fig. 6.1b, has a higher surface-to-volume ratio compared to conventional planar devices. Although a triangular Si-NW cross-section is described throughout this chapter, the modeling approach can be applied to any cross-sectional shape. The channel conductance for a device with two triangular cross-sectioned NWs operated in the depletion region can be approximated as $G_c = q\mu_b N_a L^{-1}\left(W - 2f_d/\sin\alpha\right)\left(a - f_d/\cos\alpha\right)$, with the depletion width $f_d = \left(\gamma^2 t_f^2 + 2\varepsilon_{Si}\varepsilon_o\left(V_{fg} - V_{fb}\right)/qN_a\right)^{1/2} - \gamma t_f$ (see Chapter 4 for the detailed calculation). While operated in an electrolyte, the flat-band voltage provides the connection between ψ_o and G_c, and can be expressed as $V_{fb} = E_{ref} - \varphi_{Si}q^{-1} - \psi_o - Q_f/C_{ox} - Q_{ss}/C_{ox} + \chi^{sol}$, where E_{ref} is the reference electrode potential, $q^{-1}\phi_{Si}$ is the work function of silicon, and χ^{sol} is the surface

dipole potential of the solvent. Figure 6.1c shows the potential profiles across the electrolyte to the FOX surface and the corresponding energy-band diagrams along A-A' (Fig. 6.1b, inset) with the related parameters associated with the operation of a Si-NW pH sensor. Surface reactions between the ions in the electrolyte and molecular groups on the FOX surface result in a surface charge density σ_o and surface potential ψ_o. Changes in pH_B induce a change in the surface charge $\Delta\sigma_o$ and potential $\Delta\psi_o$, which in turn induces a measurable change in the Si-NW channel conductance ΔG_c. Therefore, the sensor operation requires the consideration of three key elements that includes an ion-containing electrolyte in contact with the FOX sensing surface, and a surface charge detection method, which in this case is a multi-gate field-effect induced modulation of the NW conductance.

The bias current for conventional ISFETs and nanoISFETs is quite different (μA vs nA), and current changes with changes in pH_B have been measured differently. The $\Delta\psi_o$ of ISFETs is commonly measured with an ISFET amplifier, where the current is kept constant by modifying the E_{ref}, so that ΔE_{ref} required to maintain a constant current is the nequal to $\Delta\psi_o$ induced by pH change of the supporting electrolyte pH_B[13]. For nanoISFETs, the surface potential has been measured by maintaining a constant current[1] using an ISFET amplifier, or by monitoring threshold voltage change while scanning the front-gate at changed surface conditions[3]. We have used a different method for recording the surface potential change. A calibration curve is first recorded at pH_{pzc} by scanning the V_{fg} and recording the nanowire current i_{ds}. Then E_{ref} is set and maintained constant while measuring the current with changing surface potential, e.g. by a pH change. Each current value is then transferred to surface potential through the calibration curve, which result is a surface potential change $\Delta\psi_o$ as a function of pH_B. Compared with the threshold voltage measurement, rather than scanning the front-gating curve multiple times, a single calibration curve is required, and ψ_o can be obtained by recording the current.

A recent report has shown that using the BG to read out ΔG_c induced by ΔpH_B at the FG results in a detected sensitivity beyond the Nernst limit of 2.303λ due to a larger BOX thickness compared to the FOX thickness[3]. Considering a depletion-mode device and equating the FG nanowire conductance change with Δf_{d1} while $G_c = q\mu_b N_a L^{-1}\left(W - 2f_{d1}/\sin\alpha\right)\left(a - f_{d1}/\cos\alpha\right)$ and BG conductance change with Δf_{d2}

while $G_c = q\mu_b N_a L^{-1}\left(W - 2f_{d2}/\tan\alpha\right)\left(a - f_{d2}\right)$ with each surface initially biased near flat-band, results in $\Delta V_{bg} \approx \zeta(t_b/t_f)\Delta\psi_o$, where ζ is a geometric scaling factor that is dependent on device dimensions, and t_b is the thickness of the BOX layer. Using devices presented here results in $\Delta V_{bg} \approx 20\Delta\psi_o$, which is a huge increase in the apparent surface potential measurement. However, the Nernst theory describes the thermodynamic behavior of a surface in contact with an electrolyte and is independent from the readout method. Therefore, the Nernstian sensitivity of the nanoISFET is fundamentally limited by α, which depends on the FOX sensing surface parameters C_d and β_{int}, and the translation of $\Delta\psi_o$ into ΔG_c, which is dependent on the electrical properties of the gate-oxide/silicon interface. It should be noted that back-gating using a low-doped silicon layer, typical for commercial silicon-on-insulator wafers, is not a stable electrode material and can lead to increased noise in the surface potential measurement.

6.3 Electrolyte/SiO_2 system and the site-binding model

First, we consider the FOX surface in contact with an aqueous electrolyte solution that is hydrated to form silanol (Si-OH) surface groups, which may be positively charged, negatively charged or neutral depending on pH_B, surface composition, crystal orientation and degree of hydration. Assuming that only hydroxyl groups (OH) react with the electrolyte, the oxide surface in solution can be described by the site-binding (SB) model, which was first introduced by Yates *et al.* [17] and was later refined by Healy *et al.*[18]. The SB model uses dissociation constants of the p.d. H^+ ions and the number of reactive sites on the oxide surface to describe the relationship between pH_B and surface potential ψ_o, which represents the equilibrium between the A-OH surface sites and the H^+ ions in the bulk solution. The adsorbed H^+ ions are in contact with the oxide surface (counter-ions from the supporting electrolyte are neglected in this case), which results in a surface charge density $\sigma_o = q\left([A-OH_2^+] - [A-O^-]\right)$. Since the oxide surface can be any polarity, the number of surface sites is $N_s = [A-OH] + [A-O^-] + [A-OH_2^+]$. According to the Boltzmann distribution, the concentration of surface H^+ ions $[H^+]_s$ in the electrical double layer is related to the bulk H^+ ion concentration and surface

potential ψ_o with $[H^+]_s = [H^+]e^{-\lambda\psi_o}$ [18]. The surface deprotonation and protonation reactions can be described as

$$\text{A-OH} \rightleftharpoons \text{A-O}^- + \text{H}_\text{S}^+ \quad \Rightarrow \quad K_- = \frac{[A-O^-][H^+]_s}{[A-OH]} \tag{6.1}$$

$$\text{A-OH}_2^+ \rightleftharpoons \text{A-OH} + \text{H}_\text{S}^+ \quad \Rightarrow \quad K_+ = \frac{[A-OH][H^+]_s}{[A-OH_2^+]} \tag{6.2}$$

where K_- and K_+ are the dimensionless dissociation constants that represent the deprotonation and protonation of the A-OH sites, respectively, which are assumed to be independent of the ionization state of the oxide surface. The surface response can be linked to the bulk electrolyte using the Gouy-Chapman-Stern (GCS) model of the electrolyte double layer that forms at the FOX interface[19-21].

The GCS model describes the solution electrical double layer with a diffuse layer charge σ_{DL} starting at distance x_2 from the surface, which is the plane of closest approach for the ion centers in the solution (commonly called the Stern layer), in combination with a surface charge σ_o and potential ψ_o, respectively (Fig. 6.1c). The potential profile in the Stern layer is considered linear, resulting in $\psi_o = \phi_2 + x_2\left(\frac{8kTn^o}{\varepsilon_w\varepsilon_o}\right)^{1/2}\sinh\left(zq\phi_2/2kT\right)$, which leads to total potential across the solution

$$\psi_o = \phi_2 + \left(8kT\varepsilon_w\varepsilon_o n^o\right)^{1/2}\sinh\left(zq\phi_2/2kT\right)C_{st}^{-1} \tag{6.3}$$

where $C_{st} \approx \varepsilon_w\varepsilon_o/x_2$ is the Stern layer capacitance per unit area, z is ionic charge of the electrolyte, and n^o is ionic strength of the electrolyte[22]. The surface charge is calculated by assuming $\sigma_o = -\sigma_{DL}$ (in the absence of specific adsorption and neglecting the charge in the semiconductor layer),

$$\sigma_o = \left(8kT\varepsilon_w\varepsilon_o n^o\right)^{1/2}\sinh\left(zq\phi_2/2kT\right) \tag{6.4}$$

Combining the SB and GCS models yields the functional relationship between pH_B and ψ_o using $pH_B = pH_s - q\psi_o\left(2.303kT\right)^{-1}$, where $pH_s = -\log a_s^+$ and the surface activity a_s^+ can be found algebraically from the previous expressions, and is

$$pH_B = -\log\left\{\left[K_+\sigma_o + \left(K_+^2\sigma_o^2 + 4K_-K_+\left(q^2N_s^2 - \sigma_o^2\right)\right)\right]\left[2\left(qN_s - \sigma_o\right)\right]^{-1}\right\} - q\psi_o\left(2.303kT\right)^{-1} \tag{6.5}$$

where surface parameters N_s and C_{st} are taken from previous independent measurements of the appropriate oxide surface[17-19, 23, 24], and the equilibrium dissociation constants K_- and K_+ are estimated from the measured pH_B-$\Delta\psi_o$ data using Eqs. (6.1-6.5). The pH sensitivity of the FOX surface in contact with an electrolyte can then be analytically expressed as $\Delta\psi_o / \Delta pH_B = -2.303\lambda\alpha$, where $\alpha = \left(\xi C_d \beta_{\text{int}}^{-1} + 1\right)^{-1}$ is a dimensionless surface property that varies between zero and unity, which is dependent on a temperature dependent constant $\xi = 2.303\lambda q^{-1}$. The differential capacitance in terms of the electrical double layer potentials can be expressed as

$$\begin{aligned} C_d &= \partial\sigma_o / \partial\psi_o \\ &= \left[\left(2\varepsilon_w\varepsilon_o z^2 q^2 n^o / kT\right)^{1/2} \cosh\left(zq\varphi_2 / 2kT\right)\right] * \\ &\quad \left[1 + \left(x_2 / \varepsilon_w\varepsilon_o\right)\left(2\varepsilon_w\varepsilon_o z^2 q^2 n^o / kT\right)^{1/2} \cosh\left(zq\varphi_2 / 2kT\right)\right]^{-1} \end{aligned} \tag{6.6}$$

which characterizes the charge storing ability of the surface to surface potential changes. The intrinsic buffer capacity

$$\beta_{\text{int}} = \frac{\delta([A\text{-}OH_2^+]\text{-}[A\text{-}O^-])}{\delta pH_S} = \frac{\delta\sigma_0}{q\delta pH_S} = N_S \frac{K_b a_{H_S^+}^2 + 4K_a K_b a_{H_S^+} + K_a K_b^2}{(K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2)^2} 2.3 a_{H_S^+} \tag{6.7}$$

which is a measure of the ability of the surface to buffer small changes in the pH at the oxide surface. And the surface H^+ ion activity coefficient is

$$a_{H_s^+} = \left[K_+\sigma_o + \left[\left(K_+\sigma_o\right)^2 + 4K_-K_+\left(q^2N_s^2 - \sigma_o^2\right)\right]^{1/2}\right]\left[2\left(qN_s - \sigma_o\right)\right]^{-1} \tag{6.8}$$

From these expressions, the oxide surface sensitivity is limited to $\Delta\psi_o / \Delta pH_B \approx -58$ mV/pH at the standard temperature T = 293 K (20 °C). Analytical expressions of C_d and β_{int} can be derived using Eqs. (6.1-6.5) [21]. The modulation of $\Delta\psi_o$ with pH_B is measured as a conductance change ΔG_c in the nanoISFET due to an electric field generated across the FOX layer, which can be translated into an experimental determination of the pH_B - $\Delta\psi_o$ behavior.

6.4 Measurement setup

The depletion-mode Si-NW sensors used in this chapter are homogeneously p-type doped. Triangular Si-NWs have been fabricated with conventional microlithography, wet anisotropic etching and size reduction, oxidation, and dry etching as described in Chapter 2[14]. All devices used for solution measurements here are boron doped (N_a~6 × 10^{16} cm^{-3}) with heights h = 140 nm or 100 nm (measured with atomic force microscopy). The NW chips were oxidized at 950 °C for 15 min to form $t_f \approx$ 20 nm of gate oxide followed by a 20 min. N_2 anneal at the same temperature to reduce the Q_f. The Al contact metal was deposited and patterned to form the electrical contacts and subsequently annealed at 450 °C for 20 min. in a H_2/N_2 forming gas. Si-NW devices were then encapsulated with a 2.5 μm thick polyimide layer that have been lithographically patterned with sensing windows and contact regions open, and finally annealed at 350 °C for 1 h.

Figure 6.2 shows high-resolution scanning electron microscopy images of a representative Si-NW device used for testing. The image in the inset of Fig. 6.2a shows an example of the high-quality smooth Si-NW surfaces. Figure 6.2b shows the electrical measurement arrangement used for testing. The current of the Si-NW device was measured with a lock-in amplifier (SR830, Stanford Research Systems) with modulation frequency f = 30 Hz and v_{ds} = 0.5 V, unless otherwise mentioned. The pH calibration curves were first recorded by measuring I_{ds} while sweeping V_{fg} with a reference electrode (REF200 Ag/AgCl, Radiometer Analytical). Device chips (7 × 7 mm^2) were individually wire-bonded to a custom printed circuit board and sealed with an epoxy (Hysol M-31CL, Loctite Corp.) layer to isolate the electrical connections from the electrolyte solution (Fig. 6.2b). Following encapsulation, the devices were cleaned with UV ozone (UV/Ozone ProCleaner™ Plus, Bioforce Nanosciences) for 3 minutes to get a clean Si-NW oxide surface. Surface cleaning with UV ozone before each measurement is essential for proper device operation. The electrical conductance of the Si-NWs is optimal with short ozone treatment, not only because it results in a clean surface by removing adsorbed organic matters, but also UV irradiation anneals the oxide space charge[25]. However, prolonged exposure to UV can degrade devices by creating surface states at the FOX/Si interface[25], in our case exposure continuously > 15 min. resulted in non-functional devices. It is especially problematic for NWs as they have very large

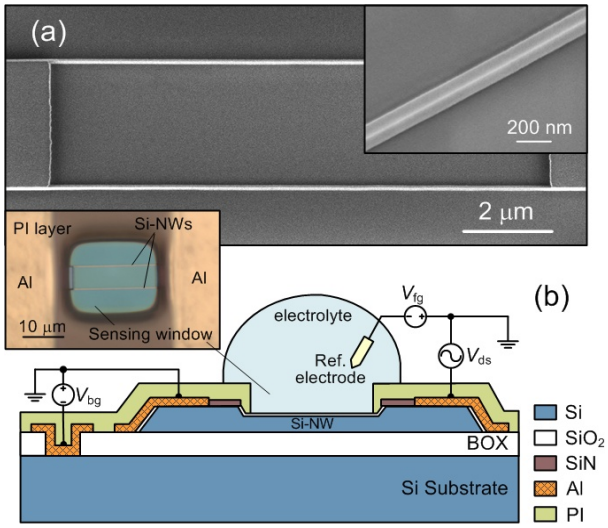

Figure 6.2 (a) High-resolution scanning electron microscopy images of fabricated Si-NWs; (b) Schematic of electrical measurement, Inset: microscope image of polyimide encapsulated device prior to testing (SiN: low-stress silicon nitride; Al: Aluminum; PI: polyimide).

surface-to-volume ratio, which makes them extremely sensitive to the interface properties. The device operation degradation, as a result of surface states, is observed by a continuous reduction of I_{ds} to zero with and applied V_{bg} and constant v_{ds}, which typically occurs within seconds. Although this kind of radiation can be reduced with low temperature annealing (e.g. 350 °C-500 °C)[26], we try to avoid this time consuming step prior to each measurement. Another commonly used surface cleaning method is oxygen plasma, however, the plasma processes were found to cause harmful radiation damage as well. Moreover, the plasma process has poor controllability due to the widely distributed plasma electron energy and the simultaneous activation of reactions[27].

Four different surfaces have been investigated in this chapter, three variations of a SiO_2 surface and an Al_2O_3 surface. First, we explore the behavior of a thermally grown SiO_2 surface, the most widely investigated ISFET surface. Three variations of SiO_2 surfaces have been investigated: a. well-cleaned SiO_2 surfaces, b. SiO_2 surfaces coated with APTES, and c. SiO_2 surfaces coated with HMDS. The APTES/SiO_2 surfaces were prepared by immersing the cleaned chip into a 1%

APTES (No. 09324, Fluka), 5% H_2O ethanol solution for 30 min., and subsequently rinsed with ethanol and dried at 120 °C in ambient air for 5 minutes. The HMDS/SiO_2 surfaces were prepared by immersing the cleaned chip into HMDS (No. 52619, Fluka) at 80 °C for 1 h and subsequently dried with N_2 flow. A FG bias voltage of $V_{fg} \approx -1.2$ V was used where the upper surfaces are moderately accumulated. The ambient measurement temperatures are indicated in their respective data plots. A pH gel electrode (PHC10101 electrode, Hach Lange) and multi-meter (HQ40D multi, Hach Lange) were used for pH measurements. The pH-meter was calibrated at pH 4.0 and pH 10.0 before each measurement at defined measurement temperatures.

6.5 Results from the SiO_2 surface

The experimental measurement of the oxide surface potential ψ_o is obtained through titration of the oxide in the presence of a supporting electrolyte. Prior to solution measurements, the Si-NW devices were immersed in the 0.1 M NaCl supporting electrolyte with 0.01 M universal buffer mixture (UBM: 0.01 M citric acid, 0.01 M phosphoric acid, and 0.02 M boric acid) solution at pH 2 for about two hours[19]. The I_{ds}-V_{fg} and g_m-V_{fg} response curves were first recorded and analyzed. The solution ΔpH_B was realized by titrating with either 1 M HCl or NaOH solution. Titration of the 0.1 M NaCl UBM buffer solution with 1M HCl and NaOH from pH 2 to 10 approximately doubles the Na^+ concentration to about 0.2 M. With C_{st} = 0.2 F m^{-2}, the differential capacitance can be estimation with $C_d^{-1} \approx 2kTq^{-1}(8\varepsilon_w\varepsilon_o kTn^o)^{-1/2} + C_{st}^{-1}$, which increases from $C_d \approx 0.16$ F m^{-2} at pH 2 to $C_d \approx 0.17$ F m^{-2} at pH 10, which corresponds to ~1% variation in $\Delta\psi_o$ for the SiO_2 surface, and even less for the Al_2O_3 surface since $\Delta\psi_o/\Delta pH_B = 2.303\lambda\alpha$, where $\alpha = \left(\xi C_d \beta_{\text{int}}^{-1} + 1\right)^{-1}$. The measured pH_B-$\Delta\psi_o$ curve was then calculated using the measured FG calibration curve. The bare SiO_2 surfaces demonstrate the well-known non-linearity for low pH values near the pH_{pzc}, which becomes more linear for pH values above about 5 (Figs. 6.3a and 6.3b) and pH_B / $\Delta\psi_o$ = 51.2 ± 3.7 mV/pH for pH range from 8 to 10. The measured I_{ds} with pH_B increases in time as shown in Fig. 6.3a. The current has been measured with the fixed V_{fg} while titrating the solution and recorded when a stable pH was reached. The ΔI_{ds} increases as pH_B

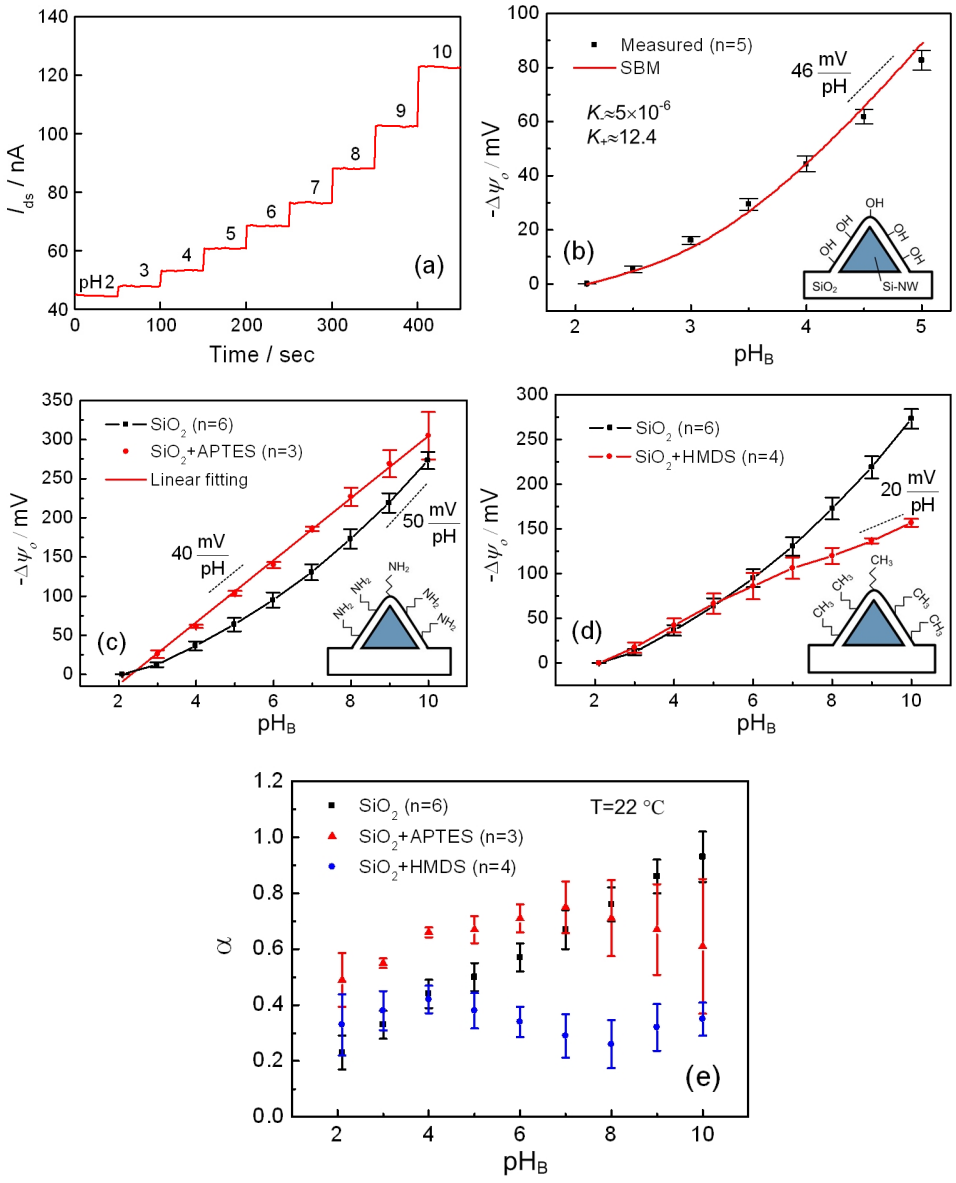

Figure 6.3 pH behavior of three SiO_2 surface variations. (a) bare SiO_2: non-linear ΔI_{ds} with increasing pH_B; (b)-(d) measured pH_B-$\Delta\psi_o$; (b) bare SiO_2: measured and fitted response (n = 5); (c) SiO_2 surfaces modified with APTES (n = 3); (d) SiO_2 surfaces modified with HMDS (n = 4); (e) Measured sensitivity parameter α for different surfaces.

is increased, which results in the non-linear response for pH values from $pH_{pzc} \approx 2$ to about 5. For a pH values greater than 5, the measured values deviate from theory due to the two-capacitor GCS model used here, which cannot describe the non-linearity of the SiO_2 surface over large pH ranges beyond about $\Delta pH_B \approx 3$[19]. Moreover, the supporting electrolyte can form ion pairs with the charged surface sites, for example, a NaCl solution can form the surface complexation $Si\text{-}O^- - Na^+ \rightleftharpoons Si\text{-}O^- + Na_s^+$ and $Si\text{-}OH_2^+ - Cl^- \rightleftharpoons Si\text{-}OH_2^+ + Cl_s^-$, which can neutralize the surface charge especially at high ionic strengths and high pH values, and will produce a lower response $\Delta\psi_o$[24]. Therefore, we have quantitatively analyzed the pH_B-$\Delta\psi_o$ response of the SiO_2 surfaces over the pH range from 2 to 5 (Fig. 6.3b). The dissociation constants from the measured data with $N_s = 5 \times 10^{18}$ m^{-2}, and $C_{st} = 0.2$ F m^{-2} [19, 24] have been estimated as $K_- = 5.0 \times 10^{-6}$ and $K_+ = 12.4$.

The dissociation constants K_- (Eq. 6.1) and K_+ (Eq. 6.2) were estimated using the combined SB-GCS model, previously reported values of C_{st} and N_s for both oxide surfaces, and the measured pH_B-$\Delta\psi_o$ data. For each ψ_o, a value for ϕ_2 was estimated from Eq. 6.4 using a numerical simplex search method. The surface charge (Eq. 6.3) was then calculated using the estimated ϕ_2. The dissociation constants K_- and K_+ were estimated from the pH_B equation (Eq. 6.5) and the measured pH_B^M. The estimation of K_- and K_+ was performed using chi-squared error minimization $\chi^2 = \sum_{i=1}^{N} \left(\frac{\left(pH_B^M, \psi_{oi}\right) - pH_B(\psi_{oi})}{\sigma_i} \right)^2$, where σ_i is the standard deviation of each measurement i. The surface ionization constants separation $\Delta pK = pK_- - pK_+$ is an important parameter to assess the pH sensing performance of the nanoISFETs where a low ΔpK translates into a high pH sensitivity due to a small amount of interference between the solution ions and H^+ ions[24]. For the bare SiO_2 surfaces, $\Delta pK \approx 6.4$, which is similar to previously reported oxide surfaces[19], however, smaller than a later report on electrolyte/insulator/silicon capacitance sensors[24]. The pH at zero surface charge is $pH_{pzc} = (pK_- + pK_+) / 2 \approx 2$, as expected. Although a three-capacitor model has been shown to fit the pH response of SiO_2 over a larger pH range from 2 to 9 [24], the two-capacitor model used in our analysis is adequate to demonstrate the nanoISFET performance. The influence of modifying the SiO_2 surface with APTES and HMDS is shown in Figs. 6.3c, 6.3d

and 6.3e, respectively. The surface pH sensitivity improves by functionalizing with APTES at $pH_B < 7$, however, reduces for $pH_B > 7$ (Fig. 6.3e). With the APTES layer, the NH_2 group is added to the oxide surface, which modifies the pH behavior. The pK_a of the amine group in bulk solution is 9, and therefore, for pH below 9, the amine group is protonated, which results in a linear pH_B-$\Delta\psi_o$ relationship, with a slope ~40 mV/pH measured from pH 2 to 10 due to the addition of surface charge from the protonated amine groups. Although $pK_a \approx 4$ have been previously measured from APTES modified SiO_2 surfaces[28], the linearization of the SiO_2 pH response near the $pH_{pzc} \approx 2$ will still occur and does not change the analysis of the measured response. The influence of modifying the SiO_2 surface with a layer of HMDS is shown in Fig. 6.3d. The reduction in surface sensitivity can be interpreted as a reduction in active silanol surface sites replaced with molecules containing methyl end groups CH_3, which are not affected in the pH ranges considered here, and subsequently the reduced active sites results in a reduced sensitivity ~20 mV/pH compared to ~50 mV/pH for bare SiO_2 surfaces. From Fig. 6.3d, the results show an approximately linear pH_B-$\Delta\psi_o$ response from pH 2-6, and a reduced sensitivity at pH values above 6, compared to a bare SiO_2 surface.

6.6 Results from the Al_2O_3 surface

Thin (15 nm) surface layers of Al_2O_3 deposited on oxidized Si-NWs have been investigated. The Al_2O_3 surface is known to have a higher pH surface sensitivity compared to SiO_2, and is more resistive to ion diffusion compared to conventional SiO_2 layers[29], which is very important for stability of the pH sensing electrode. The other gate oxides that are commonly used for pH sensing are Ta_2O_5 and Si_3N_4; both show linear and near-Nernstian pH sensitivity[20, 30, 31]. Since the pH sensitivity depends on the quality of sensing layer, the deposition technique is critical to form a high quality and uniform sensing layer[32-34], and therefore, we use ALD thin films for the pH sensing surface. The Al_2O_3 layers were deposited on oxidized Si-NWs with ALD at 300 °C (Polygon, ASM International).

Figure 6.4a shows the pH scan directions for the Al_2O_3 devices starting at $pH_B = 8$, the commonly accepted pH_{pzc} [19, 24], up to $pH_B = 10$ then down to $pH_B = 2$, and subsequently returned to $pH_B = 8$. The bidirectional scanning demonstrates negligible

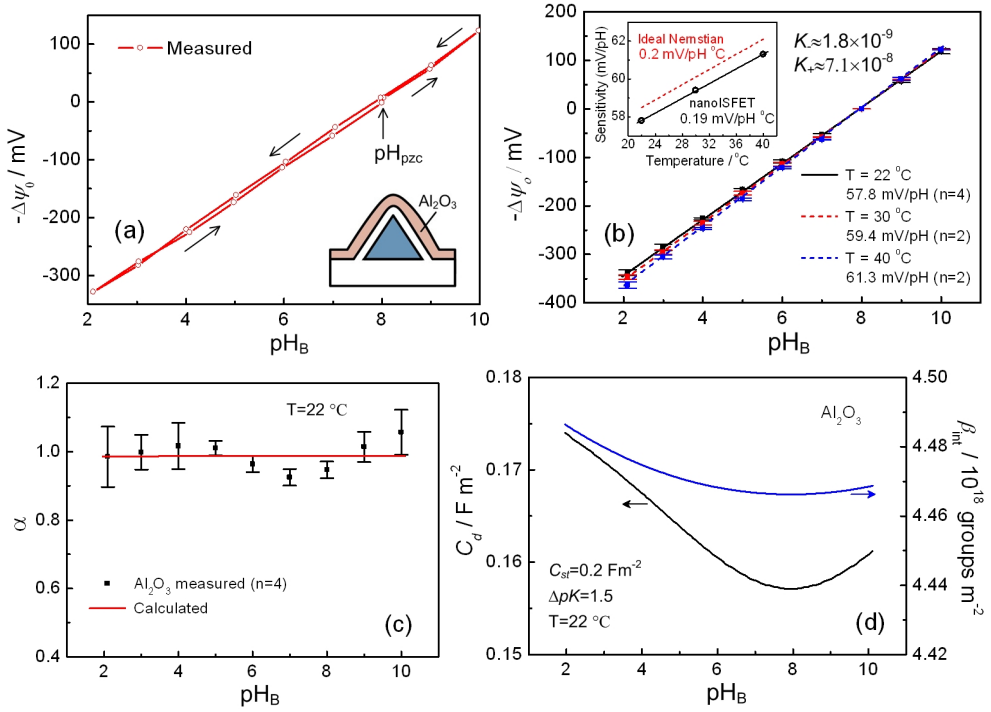

Figure 6.4 pH_B-$\Delta\psi_o$ response of ALD Al_2O_3 surfaces. (a) pH titration direction showing the response hysteresis; (b) Measured and fitted response for three different Si-NW devices at T = 22 ºC (n = 3) with $\Delta\psi_o / pH_B$ = 57.8 ± 1.2 mV/pH, at T = 30 ºC (n = 2) with $\Delta\psi_o / pH_B$ = 59.4 ± 0.3 mV/pH, and at T = 40 ºC (n = 2) with $\Delta\psi_o / pH_B$ = 61.3 ± 0.8 mV/pH; (c) Measured and estimated sensitivity parameter α (d) Estimated C_d and β_{int}.

response hysteresis. The measured pH_B-$\Delta\psi_o$ responses of the Si-NW with the Al_2O_3 FOX layer at three measurement temperatures (22 ºC, 30 ºC and 40 ºC) are shown in Fig. 6.4b, which shows a nearly ideal Nernstian response of 57.8 ± 1.2 mV/pH for T = 22 ºC, which is within experimental error of the ideal Nernstian sensitivity of 58.5 mV/pH at T = 22 ºC. The estimated dissociation constants are K_- = 1.8 × 10^{-9} and K_+ = 7.1 × 10^{-8}, using N_s = 8 × 10^{18} m^{-2} and C_{st} = 0.2 F m^{-2}. The estimated ionization constant separation $\Delta pK \approx 1.5$ is the lowest reported for an ISFET-based measurement[19, 24] and similar to values reported from titration measurements on colloidal dispersions of γ-Al_2O_3 microparticles, $\Delta pK \approx 2.2$ [35], and nanoparticles, $\Delta pK \approx 1.2$ [23]. As predicted by the estimated ΔpK of the Al_2O_3

nanoISFETs, the measured pH sensitivity of 57.8 ± 1.2 mV/pH (22 ºC) is the highest ever reported for an ISFET-based sensor with an Al_2O_3 surface at room temperature[19, 21, 34, 36-39]. Furthermore, the slope of the measured pH_B-$\Delta\psi_o$ is 59.4 ± 0.3 mV/pH at T = 30 ºC (ideal Nernstian response at 30 ºC: 60.2 mV/pH) and at T = 40 ºC the measured sensitivity is 61.3 ± 0.8 mV/pH (ideal Nernstian response at 40 ºC: 62.1 mV/pH), which also demonstrates Nernstian temperature dependence of 0.19 mV/pH ºC (ideal Nernstian response: 0.2 mV/pH ºC) (Fig. 6.4b, inset). We have assumed that the pH response isotherms intersect at pH_{pzc} = 8.

The sensitivity parameter α is plotted as a function of pH_B in Fig. 6.4c, where the solid red line represents the estimated sensitivity values, and the black markers represent the mean and standard deviation of the measured values. The measured α correlates well with the estimated values for low pH_B and has the largest deviation near the assumed pH_{pzc} with a minimum at $pH_B \approx 7$. The general behavior of α can be described by considering C_d and β_{int} (Fig. 6.4d). The differential capacitance as a function of pH_B shows a symmetric behavior with a minimum centered at pH_{pzc}[40]. The differential capacitance can also be described as the series connection of the Stern layer capacitance and the diffuse layer capacitance $C_d^{-1} = C_{st}^{-1} + C_{DL}^{-1}$. The decrease of C_d, from a maximum of 0.175 F m^{-2} to the minimum value of 0.155 F m^{-2} at the pzc, for increased values of pH_B can be explained as a decrease in C_{DL}, from a maximum of 1.4 F m^{-2} to the minimum of 0.7 F m^{-2} at the pzc ($\xi \approx 3.7 \times 10^{17}$ F^{-1} at T = 22°C), using constant C_{st} = 0.2 F m^{-2}. The density of charged surface groups β_{int} is quite large and does not significantly vary as a function of pH_B and is one of the dominant factors in the uniform and near Nernstian pH sensitivity of $\alpha \approx 1$. We attribute this high pH sensitivity to the high quality Si-NW devices and interfaces, as well as the ALD Al_2O_3 sensing layer, both of which are nearly atomically perfect, and finally FG biasing near the maximum device transconductance.

6.7 Conclusion

Silicon nanoISFETs with near atomically perfect interfaces have been presented as ultrasensitive pH sensors. Titration measurements of the nanoISFETs with SiO_2 surfaces reveal the well-known non-linear behavior for pH in the range from 2 to 5, a pH sensitivity of 51.2 ± 3.7 mV/pH in the pH range from 8 to 10. At low pH

ranges, the measured data fits well to the combined SB-GCS model of the surface ionization pH dependence with $\Delta pK \approx 6.4$. Surface modifications to the SiO_2 surface with APTES and HMDS monolayers demonstrate the ability to control the pH response by altering the surface charge density with the functional end groups of the monolayer; amine groups from an APTES layer introduce additional active ionization sites near the pzc, which linearizes the pH response and methyl groups from the HMDS layers reduce the number of active ionization sites and reduce pH sensitivity. The measured pH response of the nanoISFETs with thin ALD layers has resulted in nearly perfect Nernstian responses of pH 57.8 ± 1.2 mV/pH at 22 °C (pH range: 2-10), and in measurement temperature of 0.19 mV/pH °C (temperature range: 22 °C - 40 °C). The extracted $\Delta pK \approx 1.5$ from fitting the measured responses to the SBM further support the high pH sensitivity measurements. The NanoISFET sensors presented here provide a useful platform for pH sensing due to their simple design and fabrication with high sensitivity and reproducibility.

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Chapter 7

Integrated Lab-on-a-chip Silicon Nanowire Biosensing Platform

An integrated lab-on-a-chip (LOC) label-free biosensing platform is presented that consists of a silicon nanowire (Si-NW) biosensor chip, integrated with a microfluidic channel molded in polydimethylsiloxane (PDMS) layer for small volume sample transport. The integrated miniaturized biosensing platform is sealed with a stand-alone sample holder that combines spring-loaded electrical connecting pins that preclude the need for wire bonding and low dead volume fluidic interconnects. The functional biosensing platform is demonstrated with pH sensing experiments.

7.1 Introduction

Lab-on-a-chip (LOC) systems for the detection of biomolecules at very low concentrations are becoming increasingly important. It can provide simple, low-cost platform for applications that requiring small sample volume and high-throughput biomolecular analyses, such as protein assays for basic molecular biology research, disease marker identification, and pharmaceutical drug screening[1]. Due to the miniaturization and integration of complex functions in LOC systems, portable equipments have been realized for point-of-care/home-care testings, and have the potential to be widely applied to benefit the global public health[2].

The label-free quantification of biomolecules with biosensors is of great importance for miniaturized low-cost medical and biological applications. Currently, fluorescence detection of target-receptor binding is the most frequently used technique, although very sensitive, this method suffers from the need of target-labeling and possible alterations in target-receptor interactions caused by conformational changes or steric hindrance induced by the label[3]. For this reason, there have been considerable efforts to investigate alternatives for fluorescent detection. Surface plasmon resonance (SPR) sensing[4] is a well-established label-free technique, but requires sophisticated optical instrumentation. Electrochemical sensing as a promising technique that directly converts a biological event to an electronic signal can easily integrate with LOC system. Three commonly used characterizing technique are amperometric, potentiometric and conductometric[5]. Si-NWs as potentiometric devices measure the accumulation of charge induced potential change at the wire surface. The change of surface potential is measured based on the form of field-effect to measure pH changes, selective ion concentrations or the kinetics of biocatalytic reactions[5]. There has been a steady increase in reports of ultrasensitive sensors over the past decade based on nanoscale structures and devices such as nanowires (NWs)[6], carbon nanotubes (CTs)[7], and nanocantilever beams[8]. One-dimensional electronic structures such as NWs and CTs are particularly compelling for biosensing due to their suitability for large-scale high-density integration[9], and all-electrical readout capability. Si-NW sensors have recently attracted a large amount of attention due largely to the reported high label-free detection sensitivities of biomolecules in aqueous phase

and claims the possibility of ultimately detecting single molecules electrically in real-time[6].

In this chapter we present an integrated LOC/Si-NW biosensing platform that employs a high-yield top-down Si-NW fabrication technology combined with well-established small sample volume LOC technology thus forming a highly reliable and manufacturable platform for label-free biosensing. This platform provides wire-bonding free, automatic sampling and all-electrical signal readout functions, and can be used for the electrical detection of solution pH, and biomolecules, such as proteins and DNA.

7.2 Integrated measurement setup

7.2.1 Integrated microfluidic platform

The integrated biosensing platform consists of a Si-NW biosensing chip, microfluidic LOC for sample delivery, and a novel chip holder that seals the Si-NW and LOC chips together and provides electrical and fluidic interconnects in a stand-alone assembly. Figure 7.1 shows a schematic drawing of the integrated LOC/Si-NW biosensing platform.

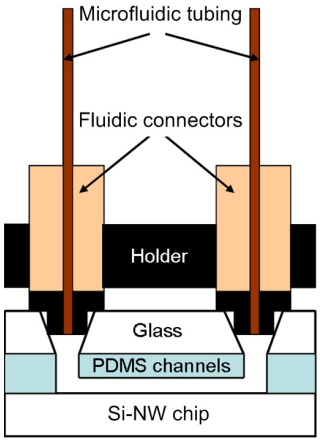

Figure 7.1 Integrated LOC/Si-NW biosensing platform with microfluidic tubing, sample inlet and outlet fluidic connectors, and three-layer integrated chip sealed with a custom-made chip holder.

7.2.2 LOC microfluidics

The LOC microfluidic chip consists of a top glass layer, a center polymer microfluidic layer made of a molded polydimethylsiloxane (PDMS) elsatomer and the bottom Si-NW chip, as shown in Fig. 7.2a. Fabrication of high-quality Si-NW devices are explained in Chapter 3. Si-NW chips (10 mm × 20 mm) are then encapsulated with 2.5 μm thick polyimide layer that have been lithographically patterned with sensing windows and contact regions open, and finally annealed at 350 °C for 1 h. The top glass (Borofloat) layer provides a solid support for attachment of the fluidic connections, and therefore, through-wafer holes are required to form the inlet and outlet ports. The through-wafer holes (1 mm top diameter) are drilled by powder blasting with 30 μm diameter alumina particles. The center microfluidic layer is a molded PDMS material, which is prepared from a silicon mold with the specified channel dimensions. The PDMS layer is 1 mm in thickness and prepared with a 10:1 mix of silicone to curing agent and cured at 70 °C. The dimensions of the microchannel in the PDMS layer are width = 50 μm, height = 50 μm, and length = 10 mm. The inlet and outlet holes for the center layer have the same diameter as the top glass layer. The PDMS and glass layers are bonded together following ultrasonic cleaning in DI water and N_2 drying. The bonded glass/PDMS chip (7 mm × 20 mm) is then aligned to the Si-NW chip using a custom alignment tool, which consists of two movable stages (*x*-*y* movable stage for Si-NW chip, and *z* movable stage for glass/PDMS chip) under a microscope. The Si-NW and glass/PDMS chips are assembled by aligning the channel with the NW sensing area on the Si-NW chips by moving the *x*-*y* stage, and then pressed together by moving the z stage after alignment. Finally the assembled chip are clamped into the custom chip holder. Figure 7.2b shows an example of an integrated LOC/Si-NW biosensing chip prior into the custom chip holder.

7.3 Results and discussion

7.3.1 Integrated LOC/Si-NW biosensing platform

The integrated LOC/Si-NW biosensing chip is clampled into the custom-made chip holder, which provides a leak-tight seal between the PDMS and Si-NW chip surfaces. The chip holder has two parts: top part and bottom part. Figure 7.3 shows

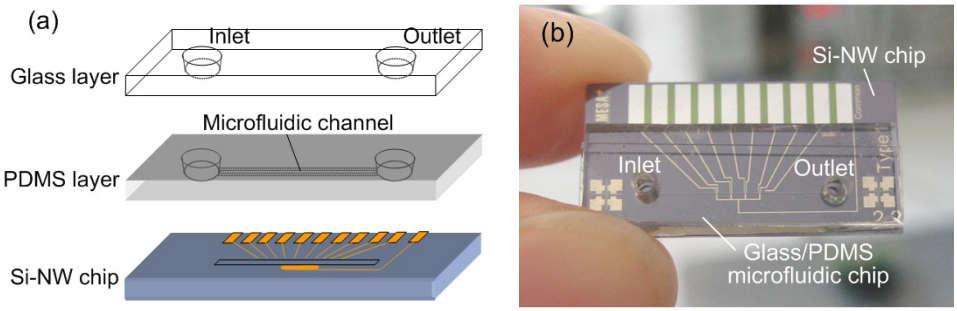

Figure 7.2 (a) Schematic and (b) real image of NW device chip assembled with PDMS and glass slide

different views of the chip holder. The top part of the chip holder (Fig. 7.3a) has a printed circuit board (PCB) connected with a spring-loaded pins (Fig. 7.3b) that contacts directly to the metal pads on the Si-NW chip to provide the electrical connection to the sensors without wire bonding. Coaxial connectors and cables are used for external electrical connections. The bottom part of the chip holder has a groove for holding the Si-NW chip assembly in place (Fig. 7.3c). The top part goes on top of the chip assembly and it is screwed to the bottom of the holder with screws to hold the chip assembly in place (Fig. 7.3d). The top part has holes tapped to fit conventional tubing holders (Nanoport, Upchurch), which was contacting the inlet and outlet holes on the chip assembly as two parts are screwed together, as shown in Fig. 7.1. Commercially available PEEK (polyetheretherketone) tubing with 360 µm outside diameter (OD) is directly connected to the Nanoport to fit the inlet and outlet ports (Fig. 7.3d). The PEEK tubing at the inlet port is connected directly to a commerically available pressure controller (MFCS-8C, Fluigent) and pressurized sample cuvettes. Si-NWs that are placed inside microfluidic channels have been shown sensitive to the flow rate[10], pulse free pumping is thus needed for reducing the noise from flow. The MFCS pressure based flow system provides an efficient pulse free pumping of solution through the microfluidic assembly, which is important for real-time biosensing and the extraction of binding thermodynamic parameters. The flow through the channel has a short response time and is stable over long duration of time. The PEEK tubing is flexible and can be easily bent to reduce the solution flow path from the reservoir to the channel, and is specially chosen as it is biocompatible, chemically inert and hence suitable for biological

sample flow. The PEEK tubing connected to the outlet port is connected directly to a waste reservoir. Serious noise has been observed by current change in Si-NWs with manual introduction of solution[11] or touching the platform with hands. Thus automatic sampling reduces the noise from the operator to the in the fluid.

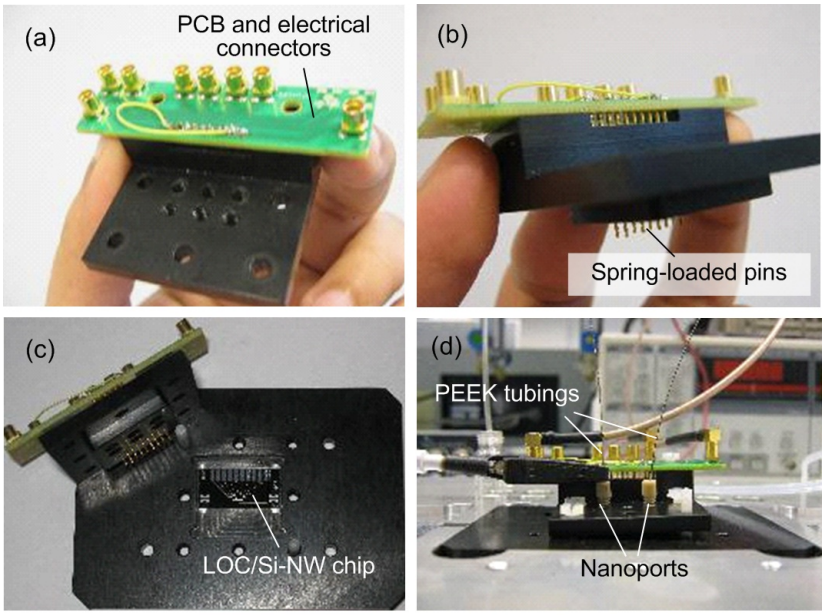

Figure 7.3 Chip holder (a-b) top (c) bottom and (d) assembled system.

7.3.2 Si-NW solution gating

The Si-NWs were characterized in solution before they were used in the integrated biosensing system. For solution measurements, a reference electrode was used as a front gate to bias the Si-NWs for all surface charge related measurements. Front gate biasing affects the depletion region differently than back-gate biasing due to the thin gate oxide and multigate behavior for the front gate. So we expect higher surface charge sensitivity for biosensing applications with this configuration[12]. Front gate conductivity modulation with a reference electrode (Ag/AgCl) in an electrolyte (100 mM NaCl) and corresponding transconductance ($\partial i_{ds}/\partial V_{ref}$, constant v_{ds}) illustrate the transition from depletion mode to depletion/accumulation mode operation as V_{ref} is scanned negative (Fig. 7.4a). The decrease in transconductance for increasing V_{ref} is due to a decrease in field-dependent effective

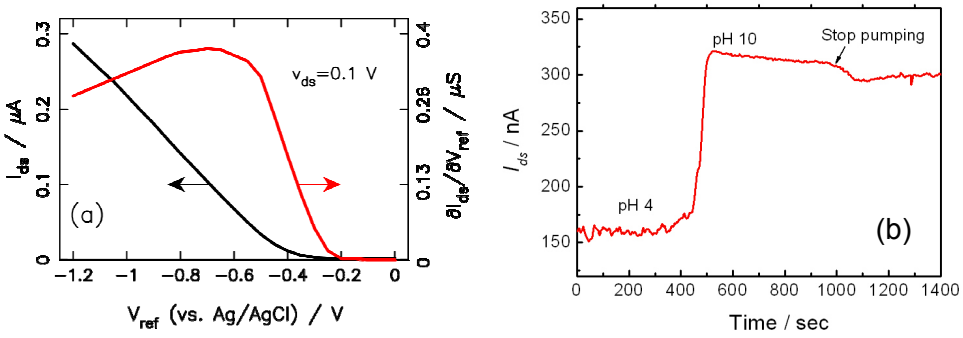

Figure 7.4 (a) Measured Si-NW front gate biasing characteristic in solution. (b) pH measurement with integrated LOC/Si-NW biosensing platform.

mobility and charge screening. For biosensing applications, the devices can be biased in the region with highest transconductance and linear i_{ds} range[12].

7.3.3 pH sensing with integrated LOC/Si-NW platform

The integrated LOC/Si-NW biosensing chip was mounted in the chip holder and clamped into position with set-screws. The PEEK tubing attached to the inlet port was connected directly to the pressurized sample cuvettes (Fluiwell, Fluigent). The cuvette was filled with 2 ml of sample buffers with different pH. The buffer solution was pumped using the pressure control system. Additional PEEK tubing was connected from the outlet port to a waste reservoir. The output PEEK tubing was sputter coated with a 1 µm thick Pt layer to serve as a pseudo-reference electrode to ensure a solution potential and to set the Si-NW bias point. Coaxial connectors and cables were used to connect the AC drain-source voltage source v_{ds} and low frequency current measurement (SR 830, Stanford Research Systems). The DC backgate voltage V_{bg} (2400 Series, Keithley) is connected to a common ground that includes the Pt electrode.

The pH sensing was done using the integrated LOC/Si-NW chip with a low frequency v_{ds}= 500 mV and DC V_{bg}=-7.5 V with respect to the Pt electrode. First, a pH 4 buffer solution was transported through the microchannel for 5 min at a flow rate of 0.5 µl/min followed by a buffer solution with pH 10 for 5 minutes and the same flow rate. The Si-NWs are p-type, and therefore, a change from pH 4 to pH 10 results in a negative surface potential change $-\Delta\varphi_o$, where $\Delta\varphi_o=\varphi_{o(pH\ 10)}-\varphi_{o(pH\ 4)}$,

which results in a reduced depletion region of the depletion-mode Si-NW devices, and therefore, an increase in the Si-NW current i_{ds}. Figure 7.4b shows an example measurement of conductance increase as the pH is changed from 4 to 10 in the integrated sensor system.

7.4 Conclusion

We have realized an integrated Si-NW biosensing chip with LOC microfluidic sample delivery system to form a label-free biosensing platform with all-electrical signal readout that is ideal for biosensing applications. The advantage of this new fabrication technique is that moderately dense arrays of Si-NWs, with precisely controlled dimensions and atomically smooth surfaces, can be directly fabricated and are compatible with conventional semiconductor manufacturing and LOC manufacturing technology. The integrated LOC/Si-NW biosensing platform offers several advantages for solution-based measurements. The new integrated sensing platform eliminates the requirement for wire bonding for electrical interconnects and sensor encapsulation for electrical isolation. The chip holder with the clamped LOC/Si-NW approach makes for a systematic, stable and leak free system for simultaneous electrical measurements with small volume transport.

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Chapter 8

Conclusions and Outlook

8.1 Conclusions

This thesis describes the work that has been done on the project "Design and optimization of silicon nanowire for chemical sensing", including Si-NW fabrication, electrical/electrochemical modeling, the application as ISFET, and the build-up of Si-NW/LOC system for automatic sample delivery.

A novel top-down fabrication technique was first presented for single-crystal Si-NW fabrication realized with a new conventional microfabrication technique. High quality triangular Si-NWs were made with high wafer-scale yield and scalable lateral dimensions down to 10 – 20 nm and lengths up to 100 μm. The thick microscale electrical contact regions formed a continuous layer of single crystal silicon, which provide an easy way for ohmic contact formation. The importance of impurity doping concentration control, ohmic contact formation, and interface charge/surface states reduction during fabrication was demonstrated with either electrical measurements or finite-element simulation. Impurity doping profile can be manipulated by the implantation dose, implantation energy, and the thermal budget. Poor ohmic contact and high contact resistance would cause device degradation and influence the electrical performance directly. The measurement results in Chapter 4 showed the Si-NW devices with ohmic contacts and low contact resistance. The channel depletion caused by the charges and states at the Si/SiO_2 interface was observed by *IV* measurements, and should be minimized by environmental control and proper annealing during the fabrication process.

In order to understand the behavior of Si-NW device in solution, an electrical/electrochemical model was developed and discussed. Both 2D analytical and 3D numerical models were developed to describe the conductance behavior of multigate Si-NW devices. The fitting of the experimental data to both models with the same dimensions and doping profiles showed the accuracy of both models. Finally, the 3D numerical model was used for the sensitivity analysis. The parameters that influence the two popular sensitivity parameters transconductance g_m and normalized conductance $\Delta G/G_o$ include the NW size, doping concentration, and gate oxide thickness were discussed in Chapter 5.

Since we are working with Si-NW sensor that are sensitive to surface potential change in solution, we first characterize the pH behavior of the Si-NW device using well established methods developed over the last 50 years for ion-sensitive field-effect transistor (ISFET) sensor. The Si-NW nanoISFET sensors were first compared with the conventional ISFET, with the advantage pointed out that nanoISFET had higher detection sensitivity due to the multigate structure. Three variations of SiO_2 gate oxide and an ALD Al_2O_3 gate oxide had been deposited on the nanoISFET and titration experiments were used to assess the pH behavior and sensitivity. The data was analyzed with the well-established site-binding model and demonstrated the near ideal Nernstian pH response of the Si-NW nanoISFET with an Al_2O_3 gate oxide.

Finally, an integrated LOC label-free biosensing platform was presented for automatic small volume sample transport and sensing. The entire platform consists of a Si-NW biosensor chip, integrated with a PDMS microfluidic channel, and a chip holder with all electrical read-out, which is ideal for biosensing application.

8.2 Outlook

8.2.1 Gate oxide

The quality and thickness control of gate oxide for Si-NWs are important for improving the stability and sensitivity. Basically, SiO_2 layer of high quality and thin is preferred in order to have leakage free oxide and high sensitivity. With high temperature oxidation step, this can be achieved easily. However, the dopant lose due to the high temperature oxidation is dramatic as shown in chapter 3. So a thin (< 5 nm) ALD oxide layer at low temperature (< 450 °C) is recommended for the

future device fabrication. Thus after forming the Si-NW structures by anisotropic wet etching, the oxide from LOCOS should be removed, then the devices go directly to the ALD deposition for forming the gate oxide.

8.2.2 Differential measurement

Based on the integrated LOC label-free biosensing platform, a differential measurement is recommended for sensitive detection of biomolecules that can eliminate the influence of unspecific binding and local environmental change. Figure 8.1 shows the electrical setup for such a measurement. The current through the sensor Si-NW i_s and through the reference Si-NW i_r are converted to voltage v_s and v_r respectively, then the differential voltage is measured by LIA. The two Si-NWs should be nearby so that they can be considered as under the same environment. The schematic of such a device for DNA detection is shown in Fig. 8.2a and the microscopy image of a real device fabricated is shown in Fig. 8.2b. The probes are immobilized on the sensor Si-NW only but not the reference one. When the sample is passing by, the target probes can then get hybridized on the sensor NW, while the unspecific binding happens to both NWs. The differential voltage measured gives the information of specific binding induced surface potential change. One of the techniques that can be used to functionalize on the sensor Si-NW and to keep the reference Si-NW free is to use the molecular printing system, which enables to print organic materials on surfaces with volumes down to a few femtoliters.

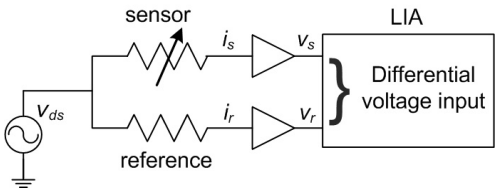

Figure 8.1 Setup for differential measurement

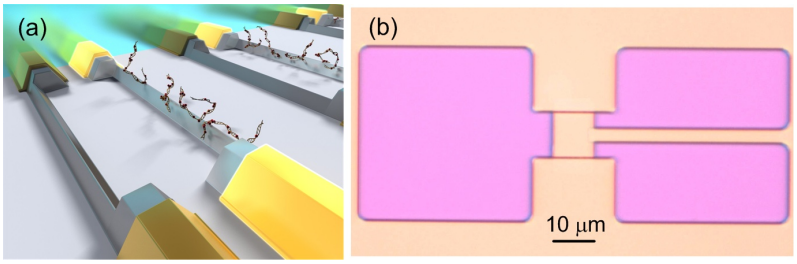

Figure 8.2 (a) Schematic and (b) microscopy image of Si-NW device designed for differential measurement

Samenvatting

Dit proefschrift is gewijd aan het werk voor het project ‘Ontwerp en optimalisatie van silicium nanodraadjes voor chemische detectie’, waaronder de fabricage van silicium nanodraadjes (Si-NW), elektrische en elektrochemische modellering, de toepassing als ISFET en de eerste stappen in de richting van een NW/lab on chip systeem voor automatische monsteraanvoer.

Een nieuwe, top-down fabricatietechniek voor de fabricatie van mono-kristallijne Si-NW met behulp van conventionele microfabricatietechnieken werd gepresenteerd. Een hoge opbrengst per wafer van goede kwaliteit driehoekige Si-NWs is behaald, met schaalbare laterale dimensies tot op 10 - 20 nm en lengtes tot 100 □m. De dikke, microschaal elektrische-contactregio’s vormen een continue mono-kristallijne laag van silicium, welke het vormen van ohmische contacten vergemakkelijkt. Het belang van het controle over de onzuiverhedendotering, het maken van ohmische contacten en het verminderen van interface lading en surface states tijdens fabricatie is gedemonstreerd aan de hand van elektrische metingen of eindige elementen simulatie. Het onzuiverhedendoteringsprofiel kan worden beïnvloed door de implantatiedosis, de implantatie-energie en het thermisch budget. Een slecht ohmisch contact en een hoge contactweerstand zorgen voor verslechtering van de NWs en beïnvloeden rechtstreeks de elektrische prestatie. De meetresultaten in Hoofdstuk 4 laten Si-NWs zien met goede ohmische contacten en een lage contactweerstand. Kanaaldepletie door ladingen en states van het Si/SiO_2-oppervlak is geobserveerd door *I,V*-metingen en kan worden geminimaliseerd door omgevingsbeheer en de juiste annealing tijdens het fabricatieproces.

Om het gedrag van de Si-NWs in oplossing te begrijpen is een elektrisch/elektrochemisch model opgesteld en besproken. Zowel het analytische 2D en numerieke 3D model zijn ontwikkeld om het geleidend gedrag van multigate Si-NWs te beschrijven. De fit van de experimentele data in beide modellen, met dezelfde dimensies en doteringsprofielen, bewees de nauwkeurigheid van de beide modellen. Ten slotte werd het numerieke 3D model gebruikt voor de gevoeligheidsanalyse. In Hoofdstuk 5 werden de parameters besproken die de twee populaire gevoeligheidsparameters, transconductantie g_m en genormaliseerde geleidbaarheid $\Delta G/G_o$, beïnvloeden, namelijk de grootte van het NW, de doteringsconcentratie en de dikte van het gate oxide.

Omdat er gewerkt wordt met Si-NW sensoren voor het verschil in oppervlaktepotentiaal in oplossing werd de meest populaire methode, pH-metingen, gebruikt om het sensorgedrag te karakteriseren. De Si-NW nanoISFET sensoren werden vergeleken met de conventionele ISFET, met nadruk op het voordeel dat de nanoISFET een hogere detectiegevoeligheid had door de multigate samenstelling. Drie variaties van een SiO_2 gate oxide en een ALD Al_2O_3 gate oxide werden aangebracht op de nanoISFET. Titratie-experimenten werden gebruikt om het pH-gedrag en -gevoeligheid te bepalen. De resultaten zijn geanalyseerd met behulp van het veelgebruikte site-binding model. Een bijna-Nernstiaanse pH-responsie van de Si-NW nanoISFET met Al_2O_3 gate oxide werd aangetoond.

Tot slot werd een geïntegreerd LOC label-free biosensing platform gepresenteerd voor het automatisch transport en detecteren van kleine volumes monster. Het gehele platform bestaat uit een Si-NW biosensorchip, geïntegreerd met een microfluidisch kanaal in PDMS en een chiphouder met een elektrische uitlezing, dat ideaal is voor de toepassing als biosensor.

Appendix

List of Symbols

C_{ox}	front gate oxide capacitance per unit area
E_F	Fermi level
E_{ref}	reference electrode potential
ε_{ox}	relative permittivity of oxide
ε_{Si}	relative permittivity of silicon
f_d	depletion width
G_c	conductance of Si-NW
g_m	transconductance
h	height of Si-NW
L	length of Si-NW
N_a	impurity doping concentration
N_s	number of surface sites
Q_f	fixed charge near Si/SiO_2 interface
Q_{it}	interface states at Si/SiO_2 interface
Q_s	depletion charge per unit area
ψ_B	potential difference between the Fermi level E_F and the intrinsic Fermi level E_i
ψ_s	silicon surface potential
ψ_o	potential at the electrolyte-insulator interface
t_b	thickness of buried oxide layer
t_f	thickness of front oxide layer
V_{fb}	flat-band voltage
V_{fg}	front-gate voltage
V_{bg}	back-gate voltage
w	width of Si-NW

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Songyue

List of Publications

Peer Reviewed Journal publications:

- **S. Chen**, J.G. Bomer, E.T. Carlen, A. van den Berg, Al_2O_3/Silicon nanoISFET with near ideal Nernstian response, *Nano Letters*, 11, 2334-2341, 2011.
- M. Masood, **S. Chen**, E.T. Carlen, A. van den Berg, All-(111) Surface Silicon Nanowires: Selective Functionalization for Biosensing Applications, *ACS Appl. Mater. Interfaces*, 2, 3422-3428, 2010.
- **S. Chen**, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, A. van den Berg, Top-down fabrication of sub-30 nm monocrystalline silicon nanowires using conventional microfabrication, *ACS Nano*, 3, 3485-3492, 2009.
- H.D. Tong, **S. Chen**, W.G. van der Wiel, E.T. Carlen, A. van den Berg, Novel top-down wafer-scale fabrication of single crystal silicon nanowires, *Nano Letters*, 9, 1015-1022, 2009.
- **S. Chen**, E.T. Carlen, A. van den Berg, Design and modeling of multi-gate silicon nanowire devices, in preparation.

Patent:

- A. van den Berg, J.G. Bomer, E.T. Carlen, **S. Chen**, R.A. Kraaijenhagen, H.M. Pinedo, Method for manufacturing a single crystal nano-wire, WO 2011/019282 A1.

International Conferences:

- **S. Chen**, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, A. van den Berg, pH sensitivity of single crystal silicon nanowires, Materials Research Soceity (MRS 2009), Fall Meeting, Boston, MA, U.S.A, 2009. (**Oral presentation**).

- **S. Chen**, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, and A. van den Berg, Top-Down Fabricated Single Crystal Silicon Nanowires for Biosensing, Nano Bio Tech Conference, Montreux, Switzerland, 2009. (**Best poster prize**)
- **S. Chen**, J.G. Bomer, W.G. van der Wiel, E.T. Carlen, A. van den Berg, Simple top-down fabrication of single crystal silicon nanowires, Materials Research Soceity (MRS 2009), Spring Meeting, San Francisco, CA, U.S.A, 2009.